

# Orta Block Diagram

Project code: 91.4U101.001  
PCB P/N : 48.4U101.0SA  
REVISION : 06245-SB

## PCB Layer Stackup

L1: Signal 1  
L2: VCC  
L3: Inner Signal 2  
L4: Inner Signal 3  
L5: GND  
L6: Signal 4

## CPU V\_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

## SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

## SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

## SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

## SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	ID2V_S5 2D5V_S0 ID5V_S0

## SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

## Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

**wistron**

Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

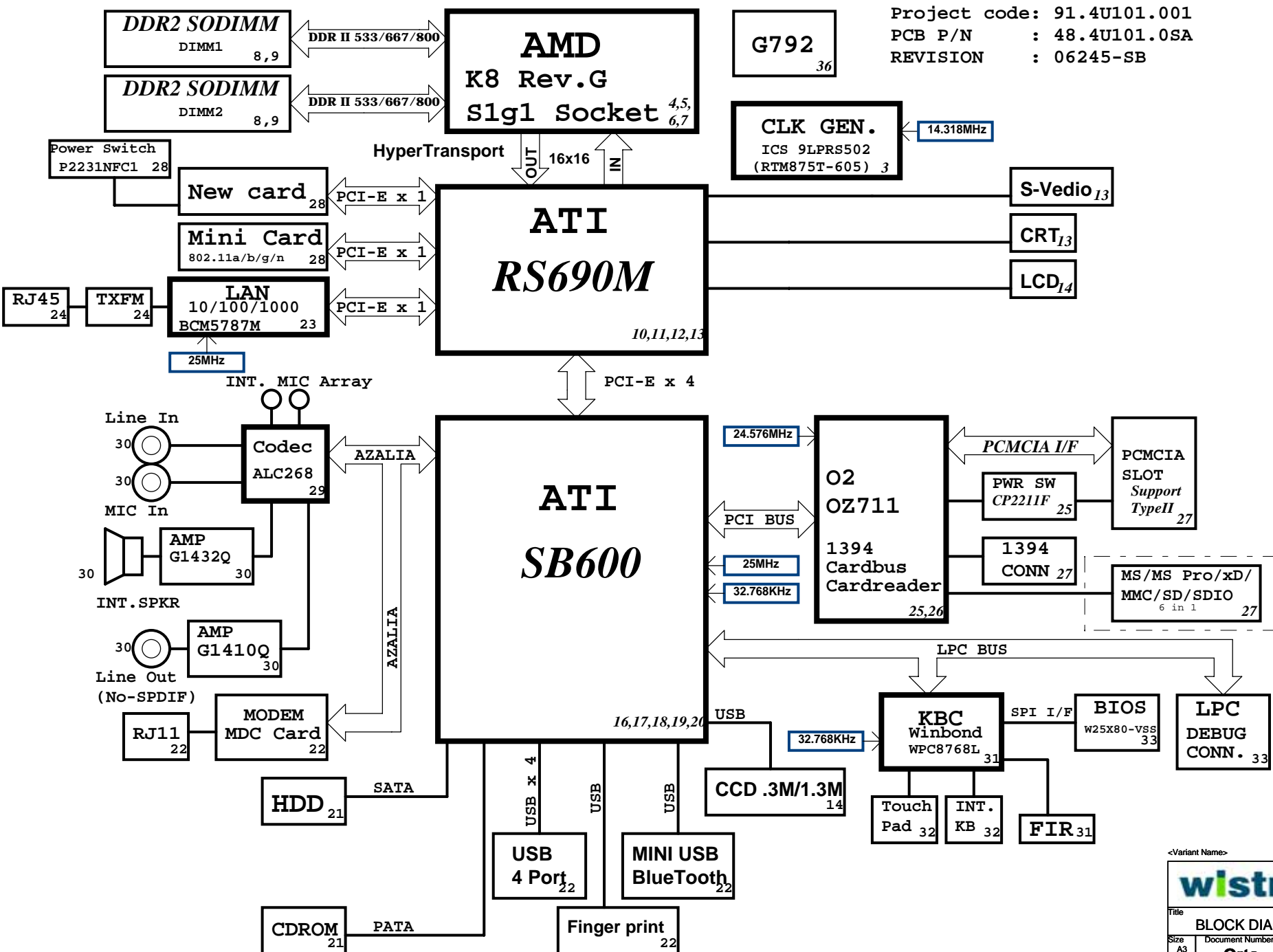
Title  
**BLOCK DIAGRAM**

Size A3 Document Number

Date: Friday, January 12, 2007

Sheet 1 of 46

Rev SB



SA: 07/31/06 Start

SB change  
power team  
1.change L7, L9 to 68.1R510.10D  
2.changge U12 to 84.04706.037  
3.change R66 to 10K ohm

<Core Design>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CHANGE HISTORY

Size

Document Number

Rev

A3

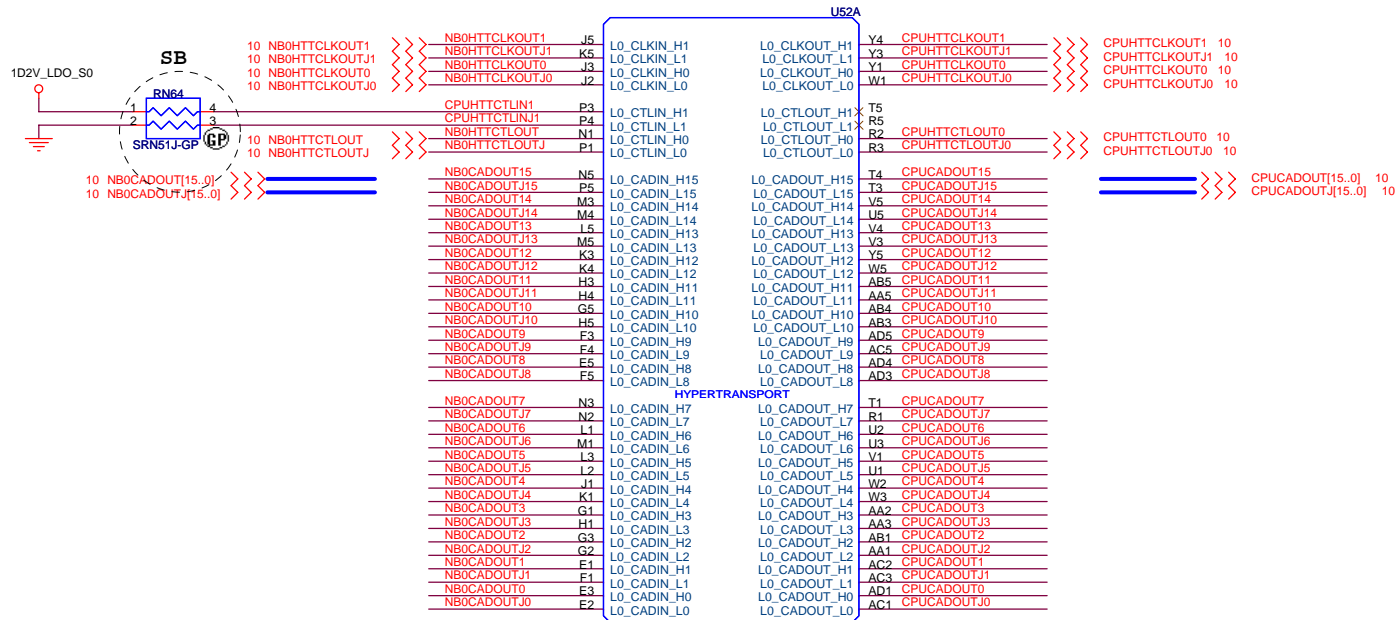
Orta

SB

Date: Friday, January 12, 2007

Sheet 2 of 46



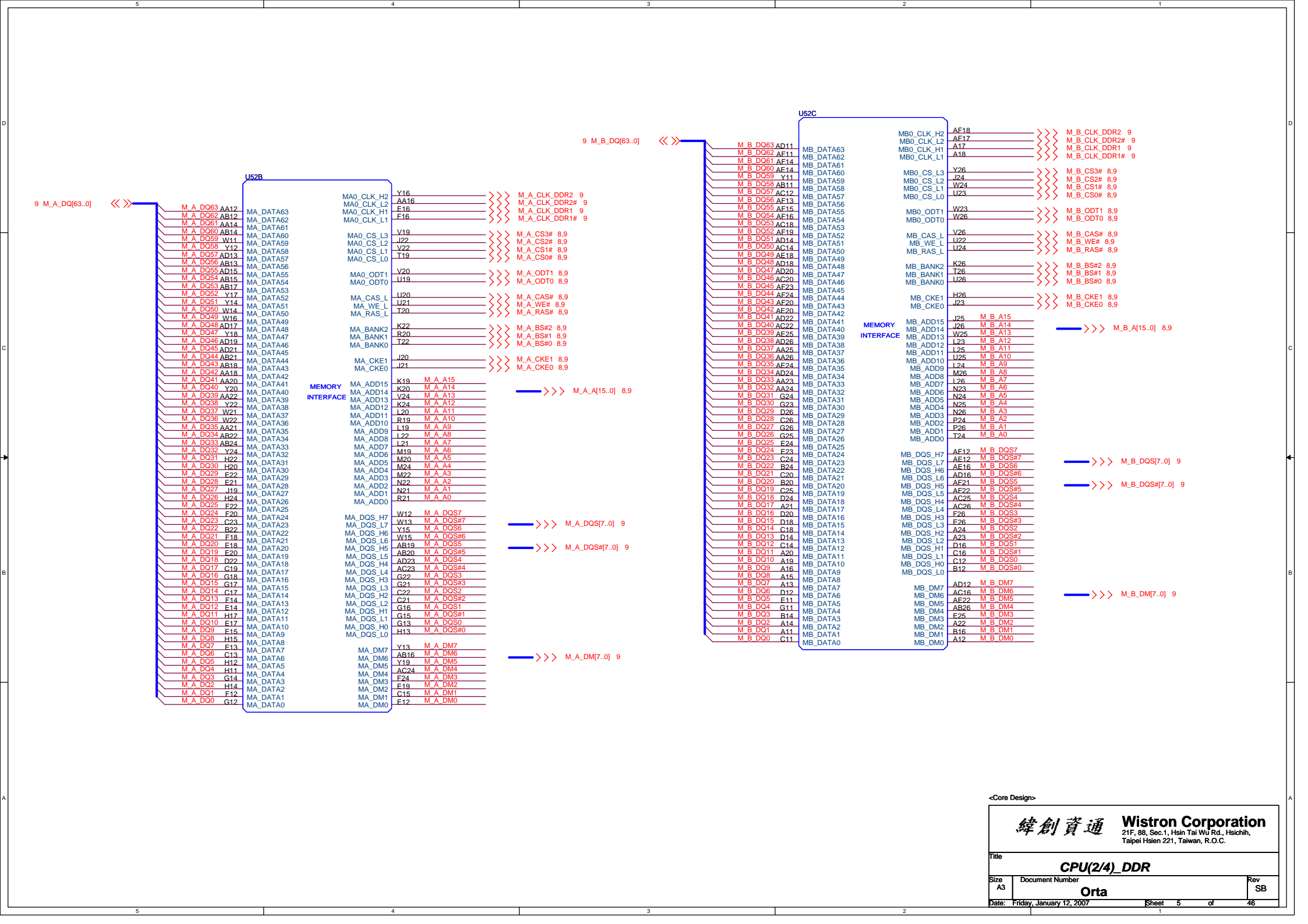


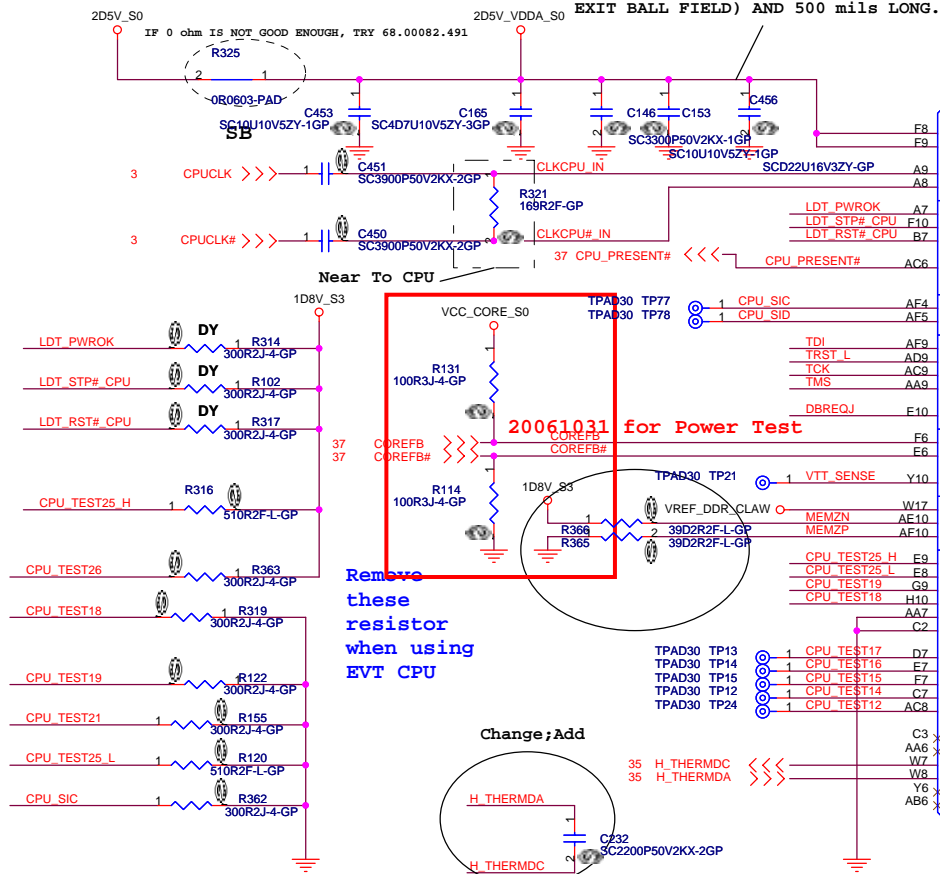
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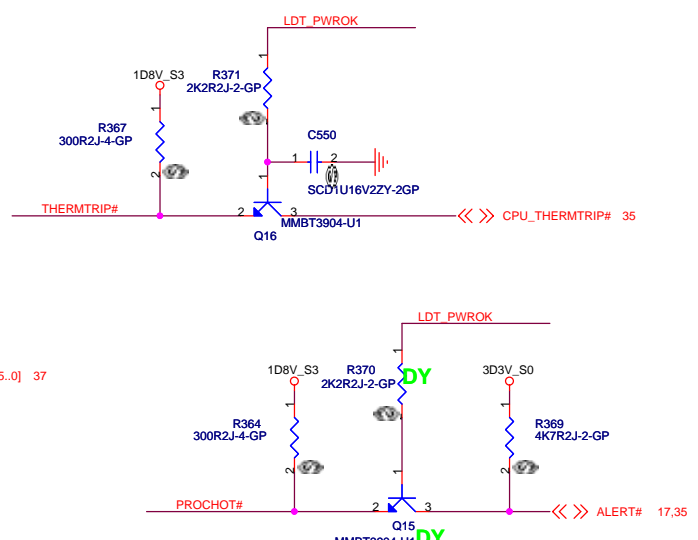
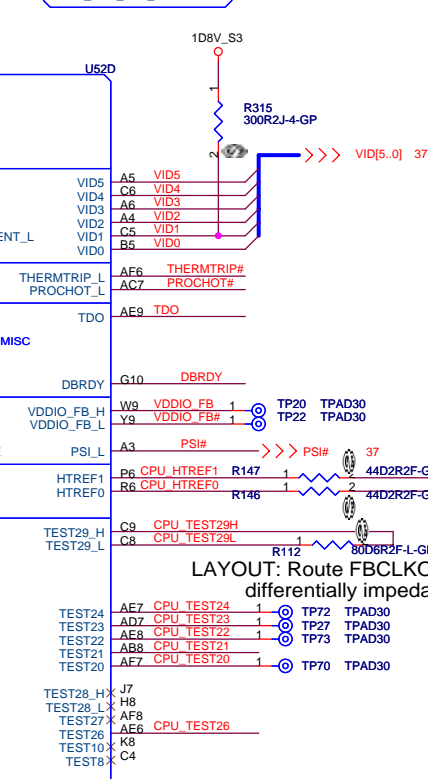
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU(1/4)_HyperTransport I/F		
Size	Document Number	Orta			Rev
A3					SB
Date:	Friday, January 12, 2007	Sheet	4	of	46

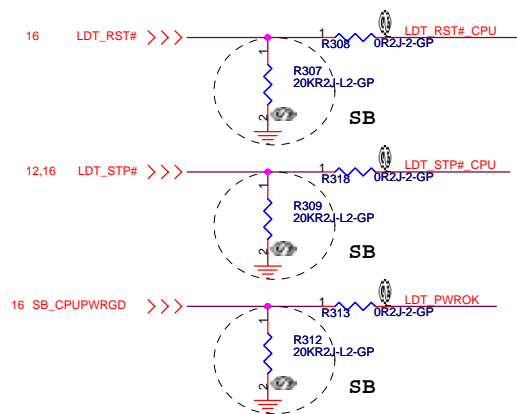
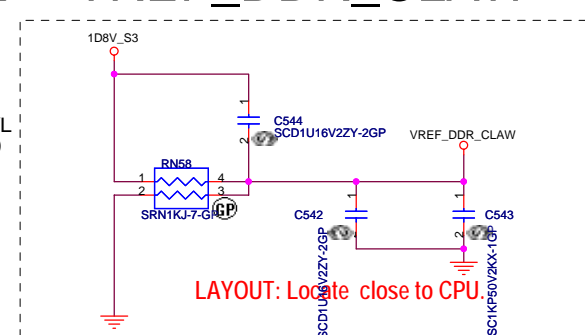


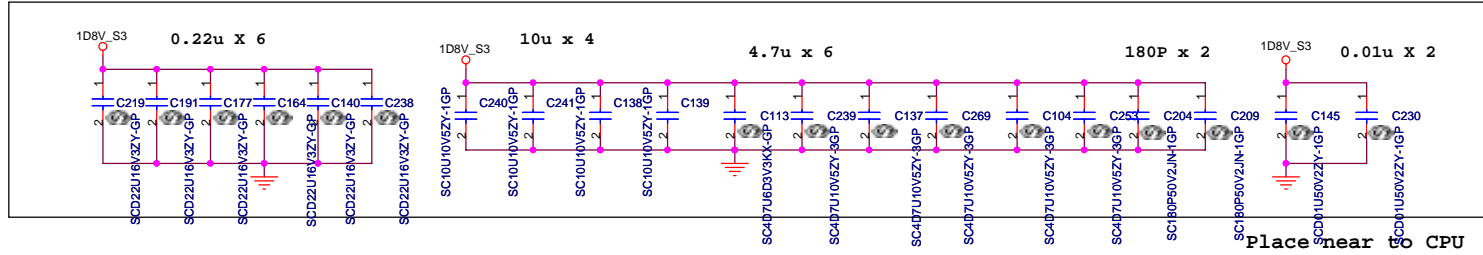
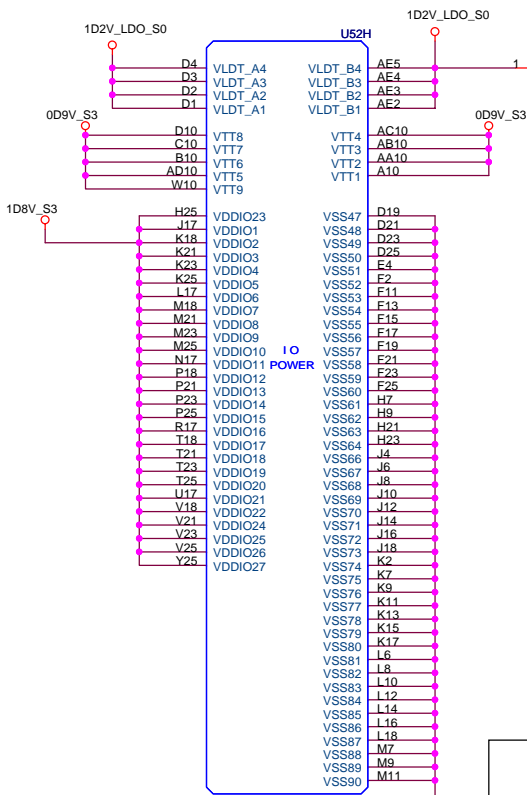


		U52E		
P20	*RSVD_MAO_CLK_H3	RESET_LX	H16	
P19	*RSVD_MAO_CLK_H3	RESET_LX	B18	
N20	*RSVD_MAO_CLK_H0			
N19	*RSVD_MAO_CLK_L0	VIDSTRB1	B3	
		RSVD_VIDSTRB0	C1	
	RSVD_VDDNB_FB_HX		H6	
	RSVD_VDDNB_FB_LX		G6	
	RSVD_CORE_TYPEX		D5	
	MISC			
	INTERNAL	FREQ5	R24	
		FREQ6	W18	
R26	*RSVD_MBO_CLK_H3	FREQ4	R23	
R25	*RSVD_MBO_CLK_L3	FREQ3	A48	
P22	*RSVD_MBO_CLK_H0	FREQ2	H18	
R22	*RSVD_MBO_CLK_L0	FREQ3	H19	

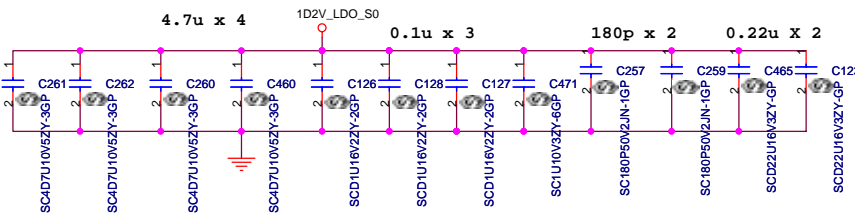
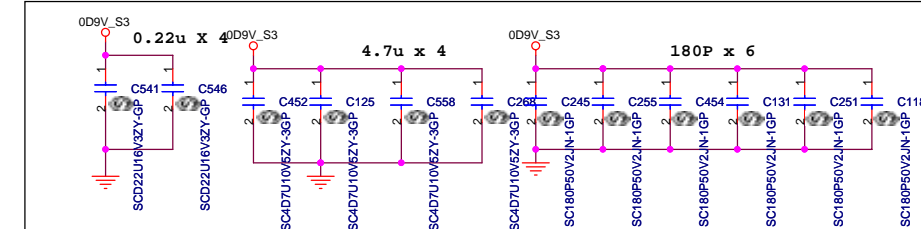
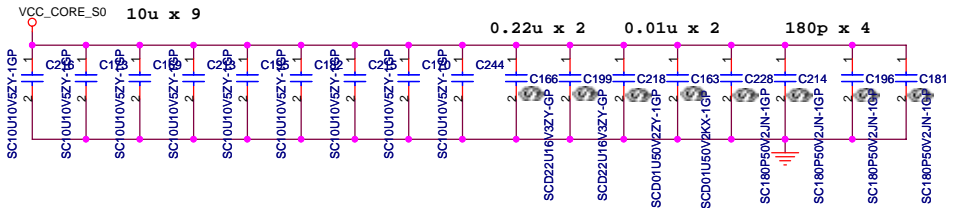


# VREF DDR CLAW





LAYOUT: Place on backside of processor.



<Core Design>

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Title		Rev
CPU(4/4)_Power		
Size A3	Document Number	SB
Date: Friday, January 12, 2007		Sheet 7 of 46



# NORMAL TYPE

# NORMAL TYPE

DDR\_VREF

LAYOUT: Locate close to DIMM

High 9.2mm

Hi 9.2 mm High 5.2mm  
Main Source: 62.10017.A61

<Core Design>

緯創資通

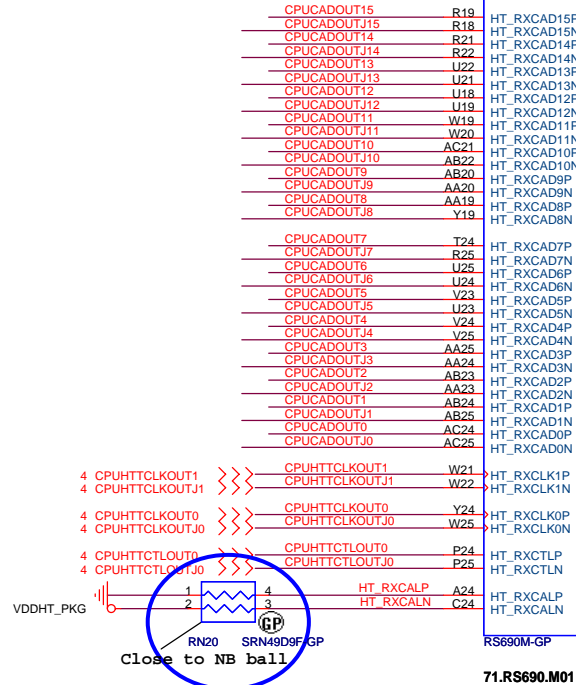
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21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,  
Taipei Hsien 221, Taiwan, R.O.C.

DDR SO-DIMM SKT

File	Document Number	Rev
Size	Custom	SB
Date: Friday, January 12, 2007	Sheet 9 of 46	

## CLAW HAMMER TO NB

4 CPUCADOUT[15..0] >>>  
4 CPUCADOUTJ[15..0] >>>



## NB TO CLAW HAMMER

HYPER TRANSPORT CPU  
I/F



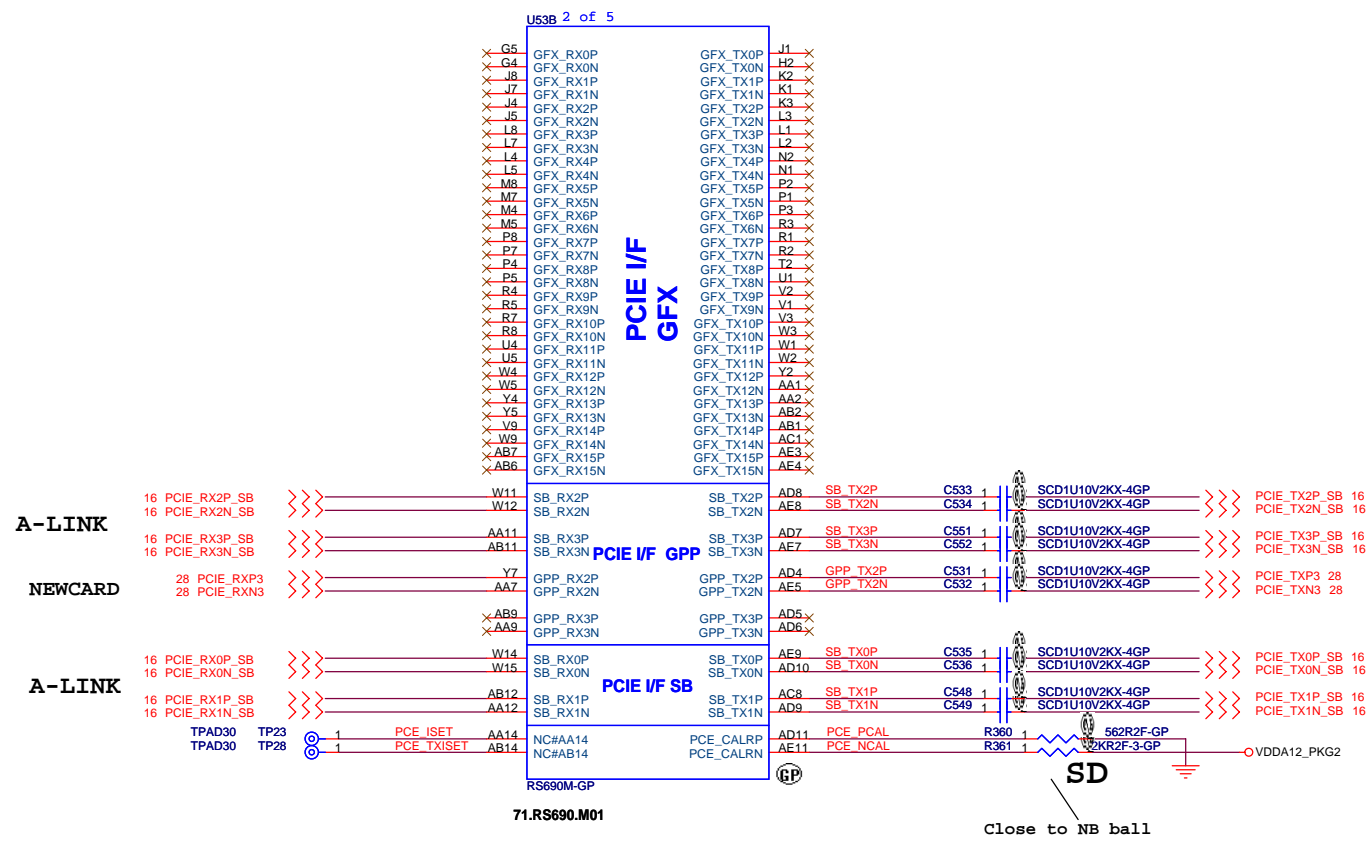
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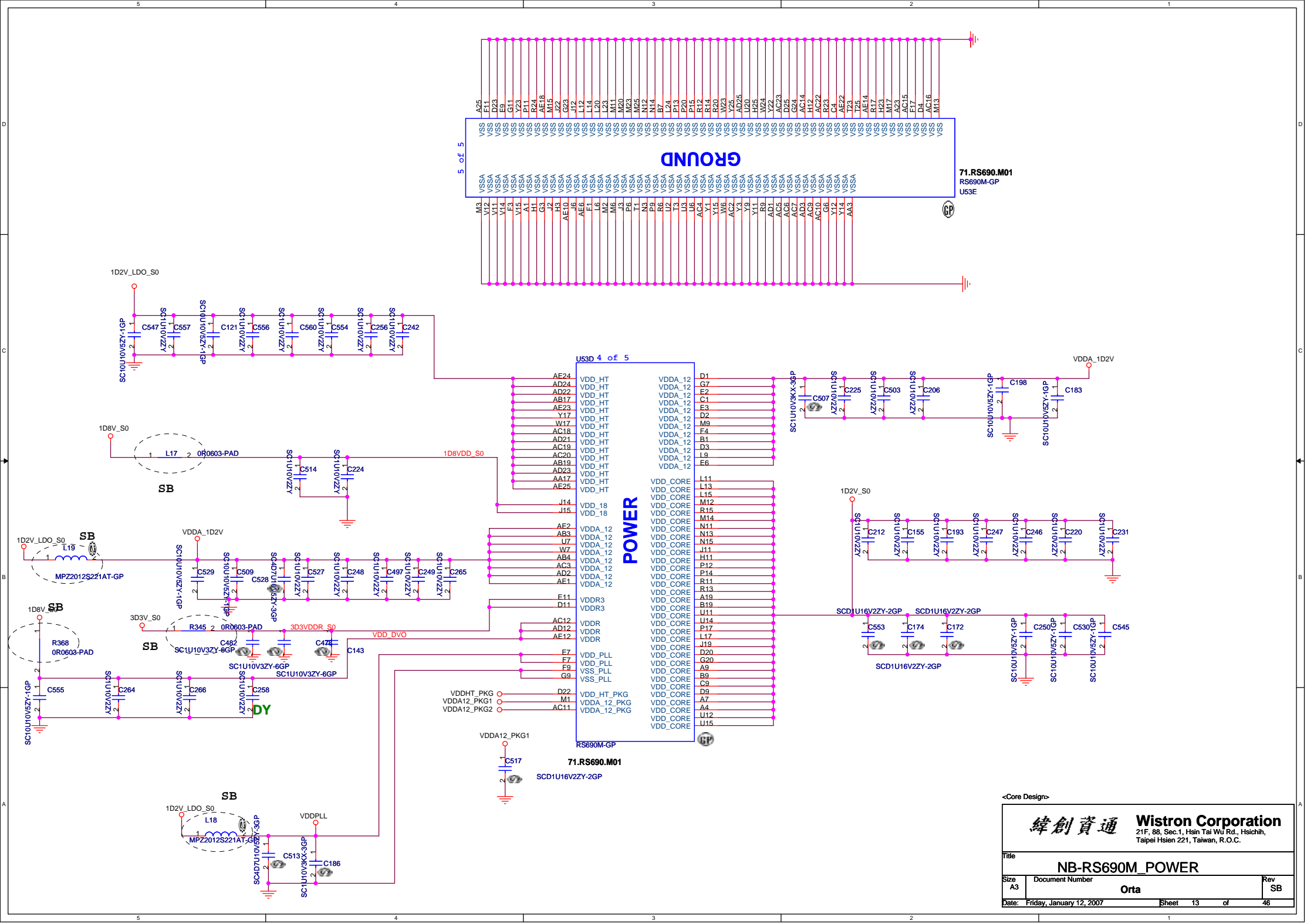
Wistron Corporation

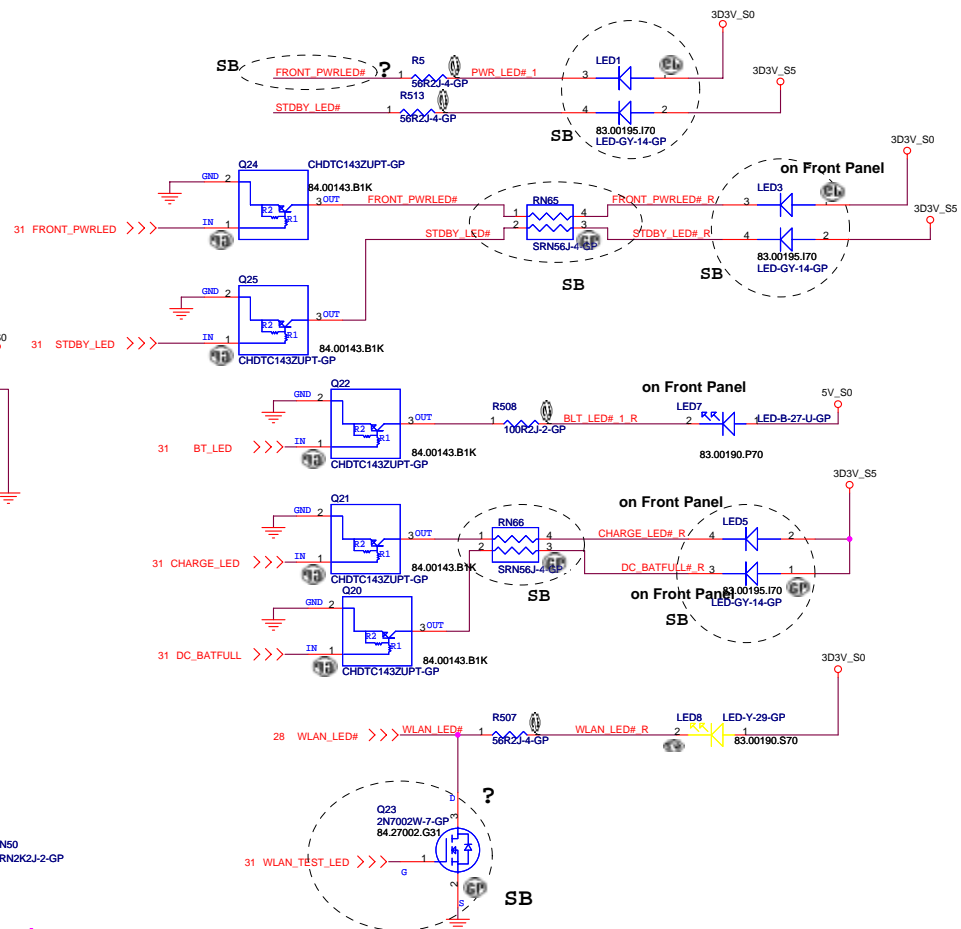
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

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Size	Document Number	Orta		Rev
A3				SB
Date:	Friday, January 12, 2007	Sheet	10 of 46	

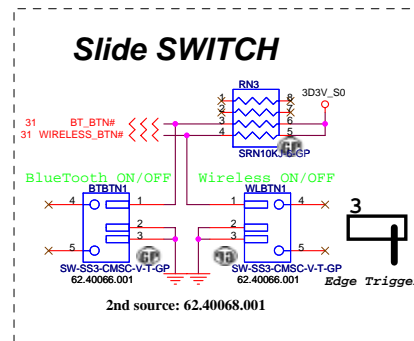








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2nd source: 20.K0185.008

3D3V\_50

EC23 100nF

R23 10k

LEDB1 20.K0185.008

1 2 3 4 5 6 7 8 9 10

20.K0228.008

ACES.COM 5-GP

SC1K50/2XX-GP

EC24 100nF

EC25 100nF

EC26 100nF

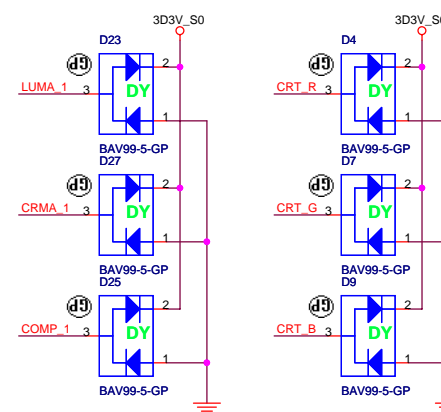
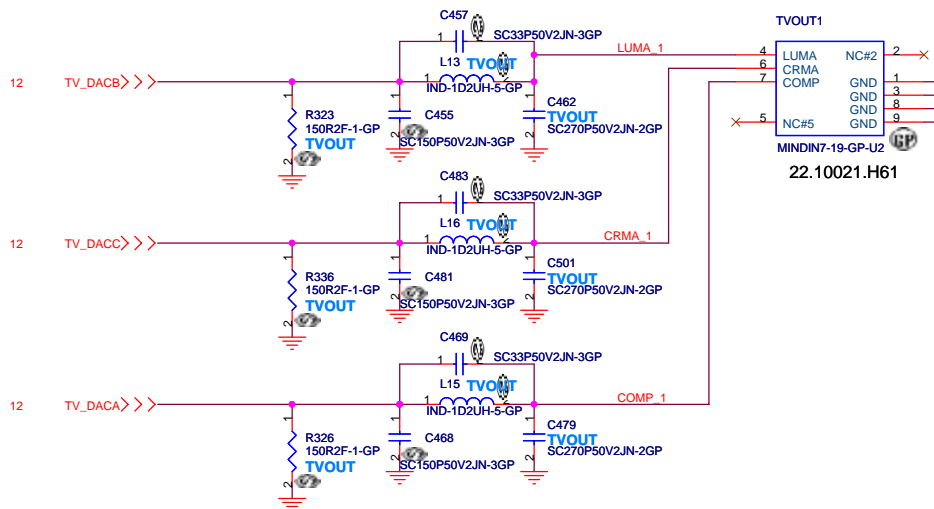
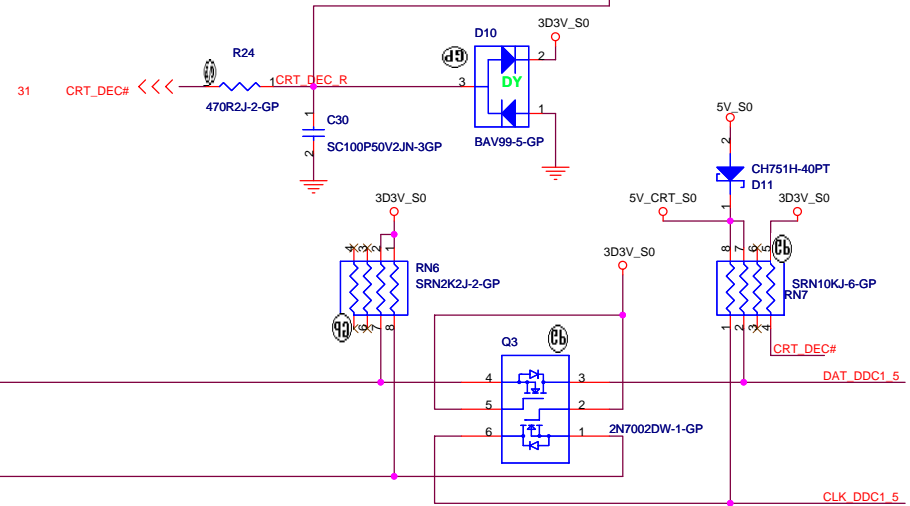
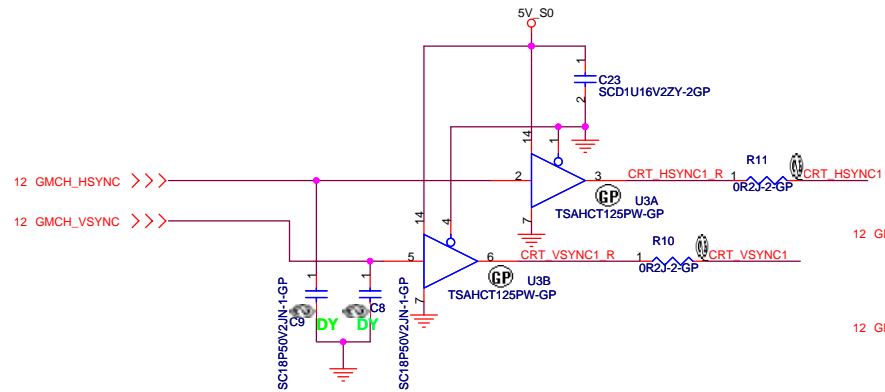
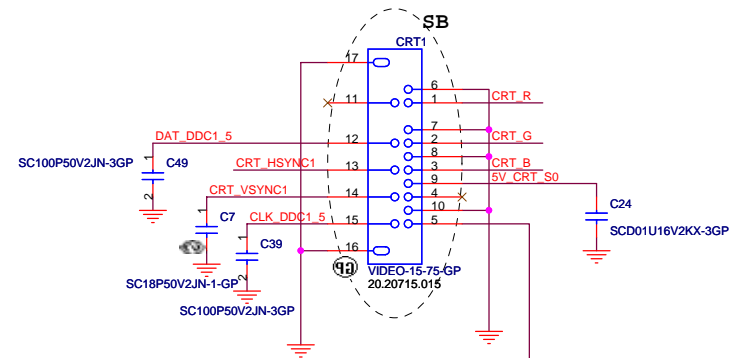
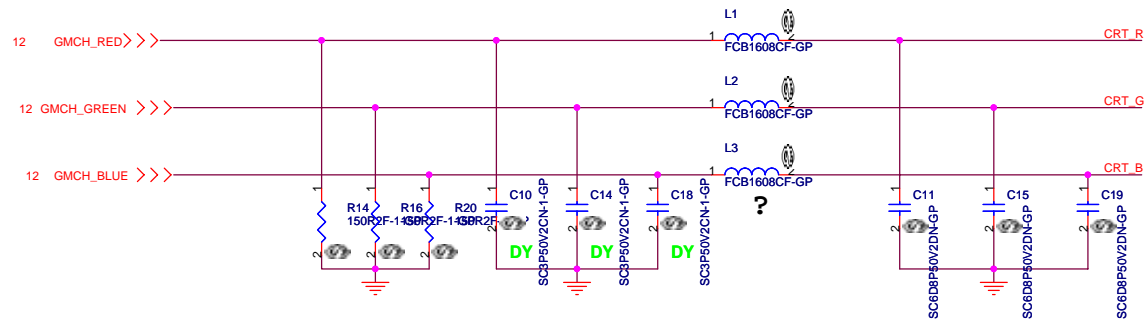
3D3V\_50

31 31 31

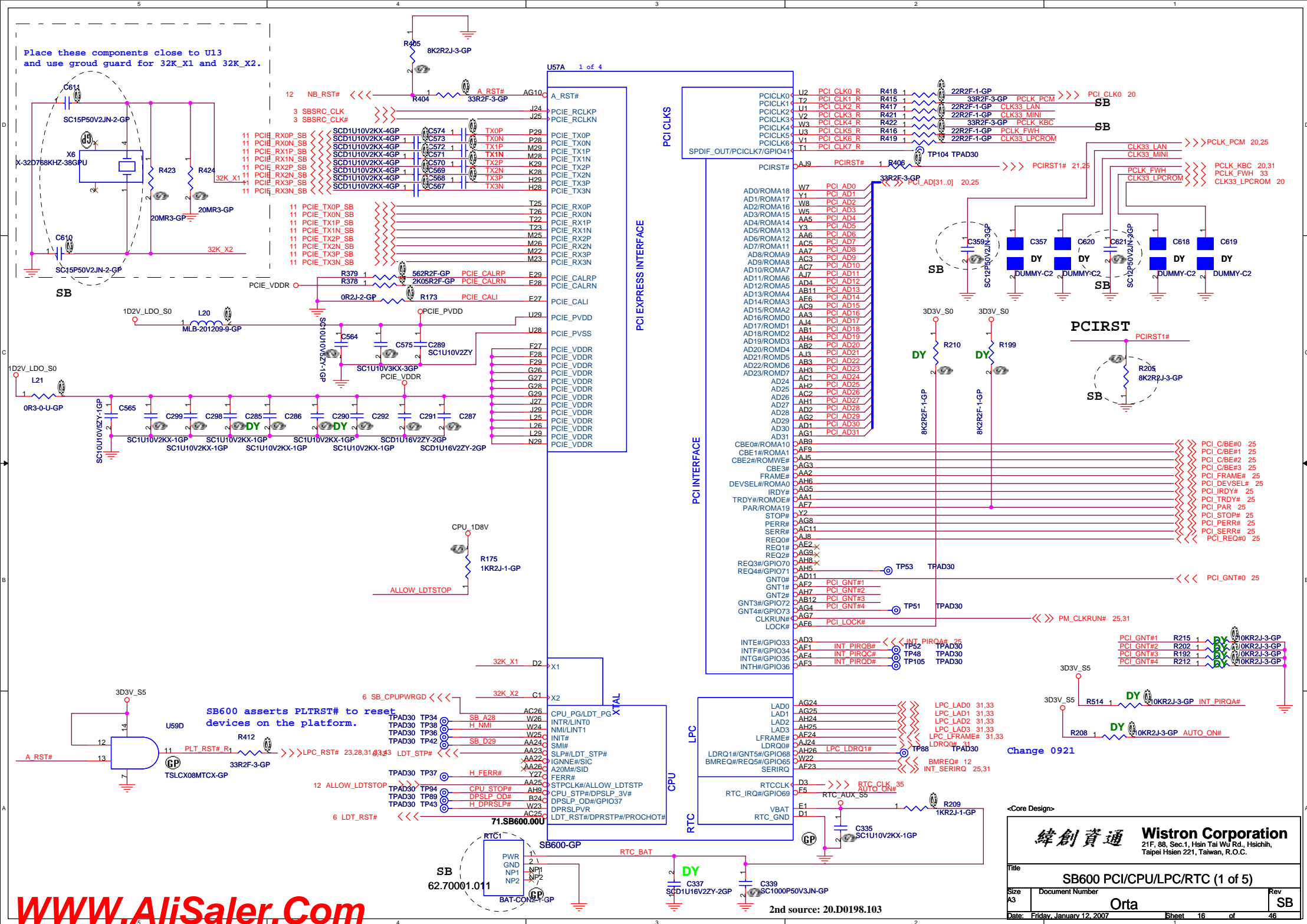
CAP\_LED# 31


NUM\_LED# 31

MEDIA\_LED# 31



Place these components close to U13  
and use groud guard for 32K\_X1 and 32K\_X2.

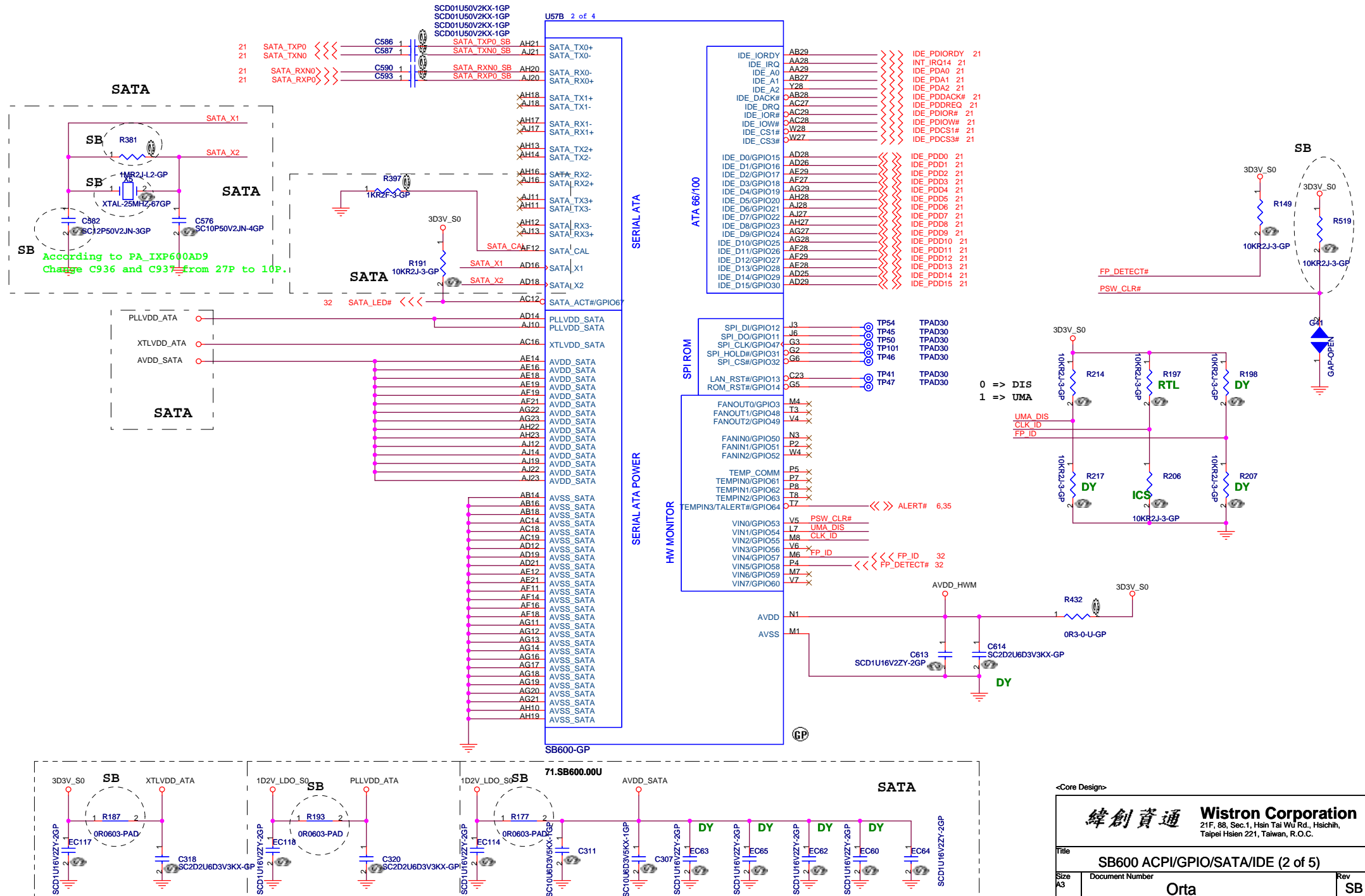


 <b>緯創資通</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
SB600 PCI/CPU/LPC/RTC (1 of 5)	
Size A3	Document Number
	Orta
Date: Friday, January 12, 2007	Rev
	SB
Date: Friday, January 12, 2007	Sheet 16 of 46

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**2nd source: 20.D0198.103**

PLACE SATA AC DECOUPLING  
CAPS CLOSE TO SB460



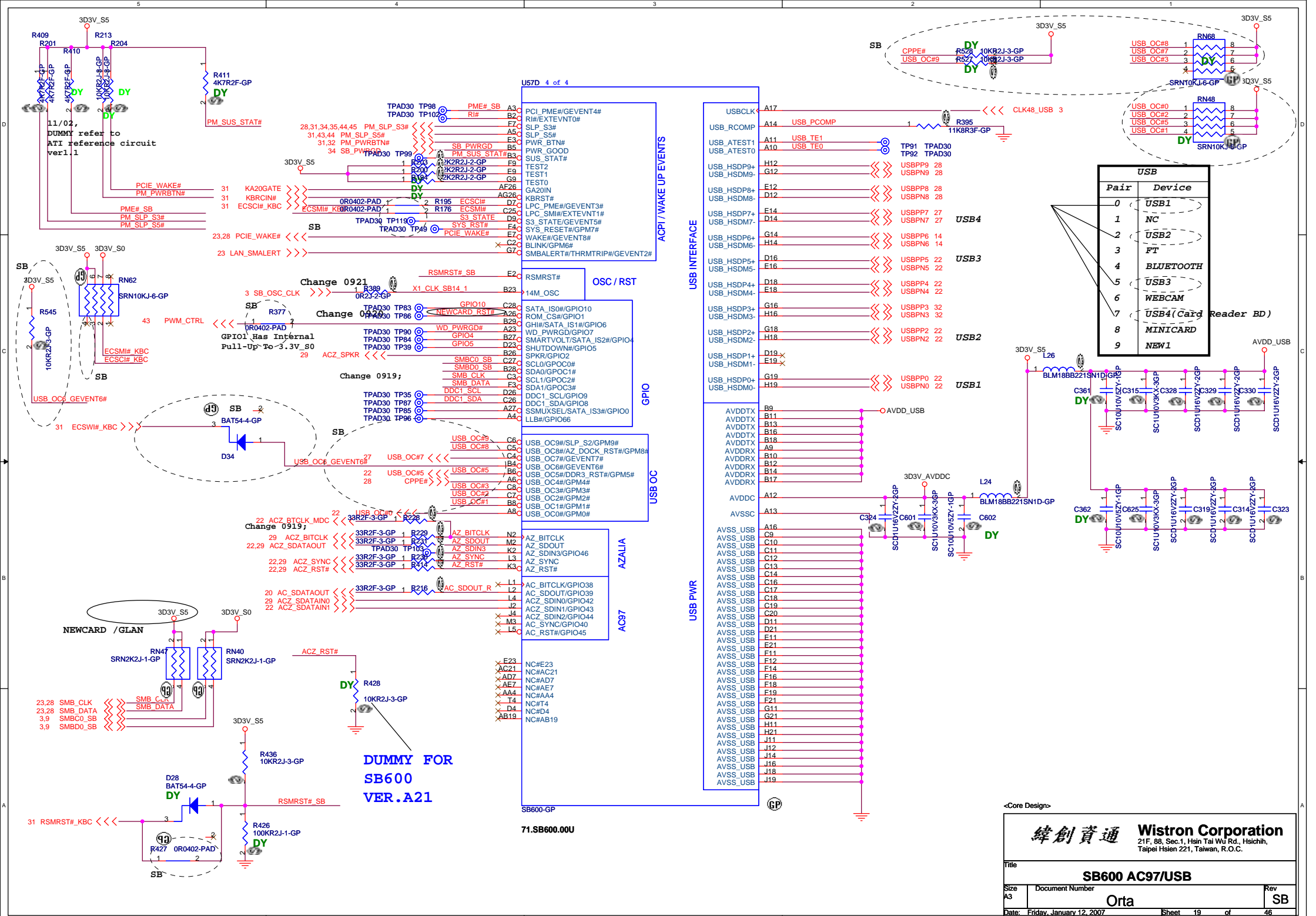
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**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title	SB600 ACPI/GPIO/SATA/IDE (2 of 5)
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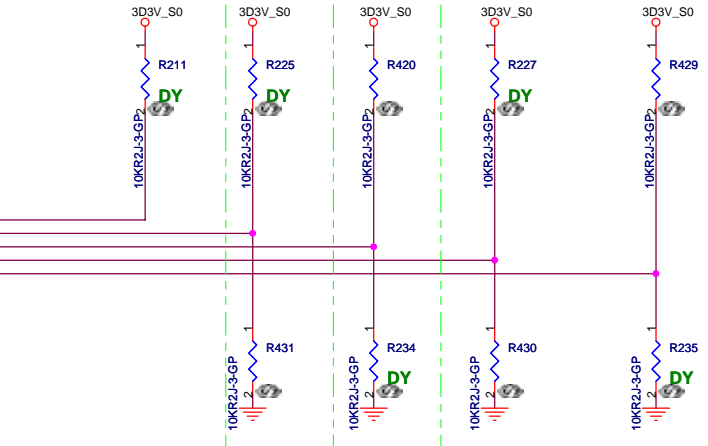
Size A3	Document Number <b>Orta</b>	Rev <b>SB</b>
Date: Friday, January 12, 2007	Sheet 17 of 46	





PCI\_CLK4  
PCI\_CLK6  
PCI\_CLK0  
PCI\_CLK1

19 AC\_SDATAOUT  
16,31 PCLK\_KBC  
16 CLK33\_LPCROM  
16 PCI\_CLK0  
16,25 PCLK\_PCM

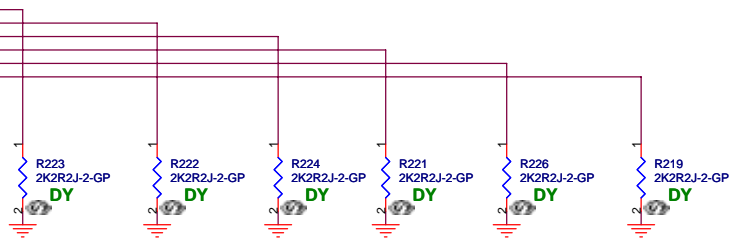


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[23..28]

16,25 PCI\_AD28  
16,25 PCI\_AD27  
16,25 PCI\_AD26  
16,25 PCI\_AD25  
16,25 PCI\_AD24  
16,25 PCI\_AD23



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

緯創資通

Wistron Corporation

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Title

SB600 STRAPPING PIN

Size

A3

Document Number

Orta

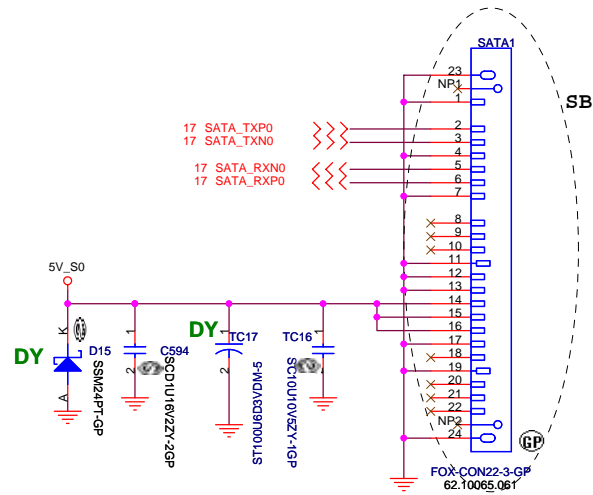
Rev

SB

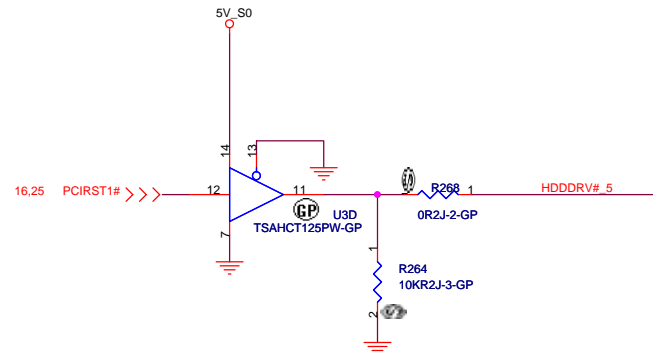
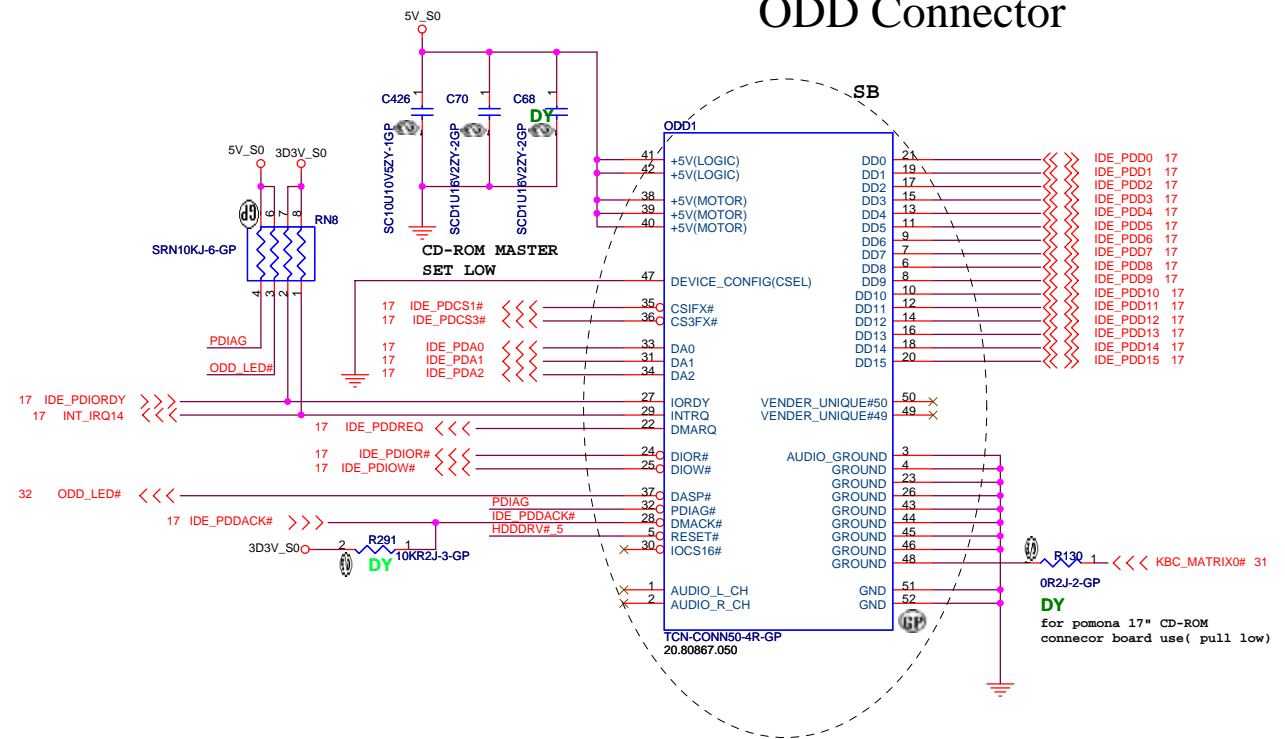
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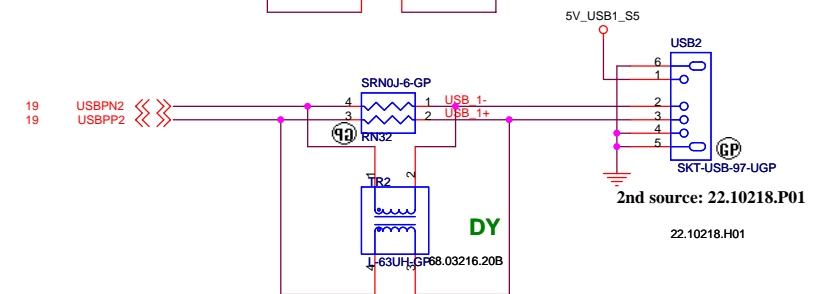
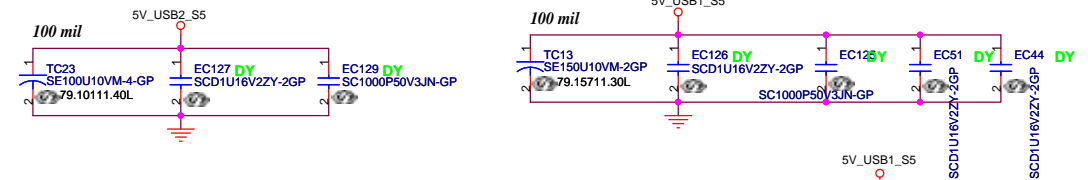
Sheet 20 of 46

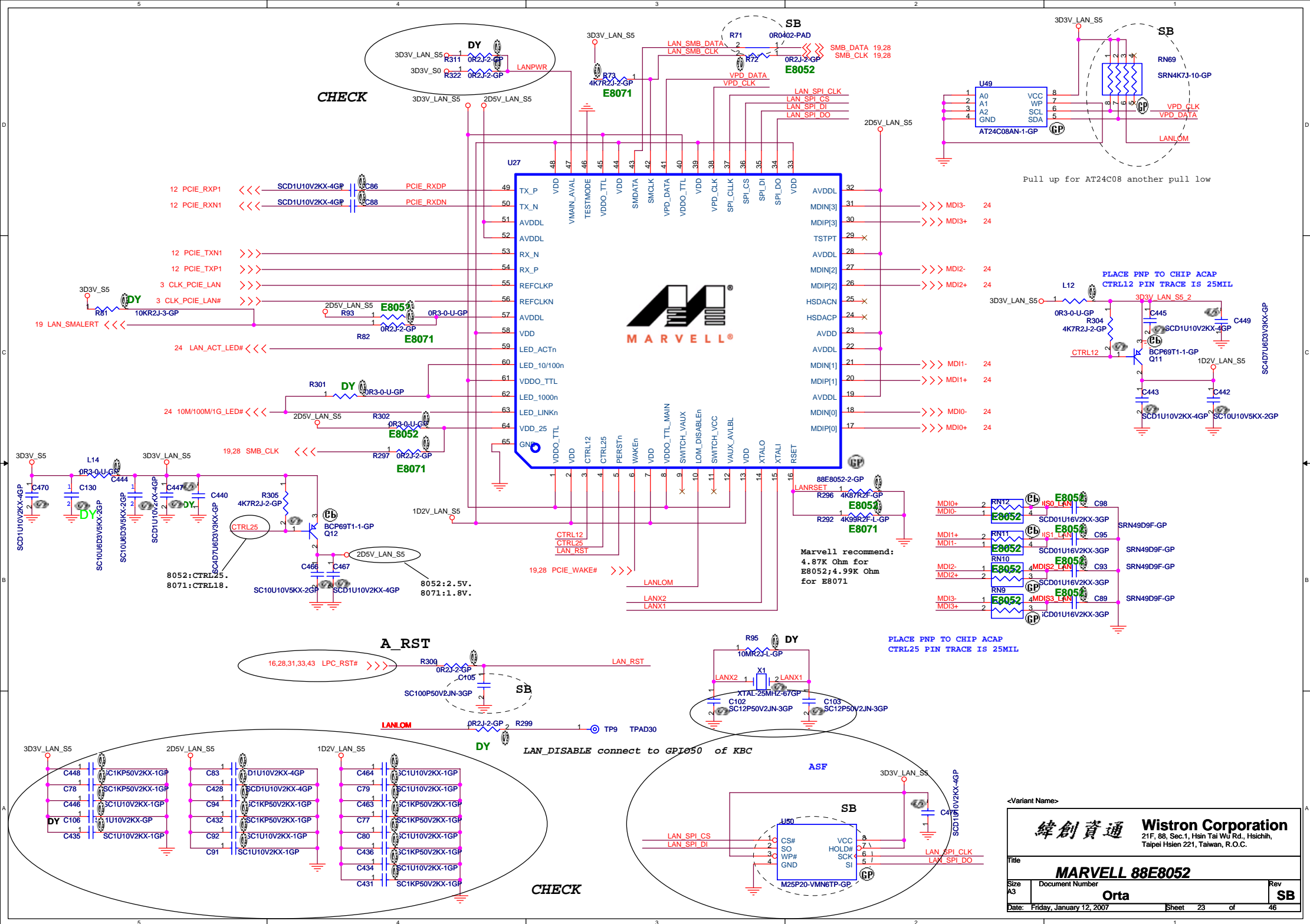
## SATA HD Connector



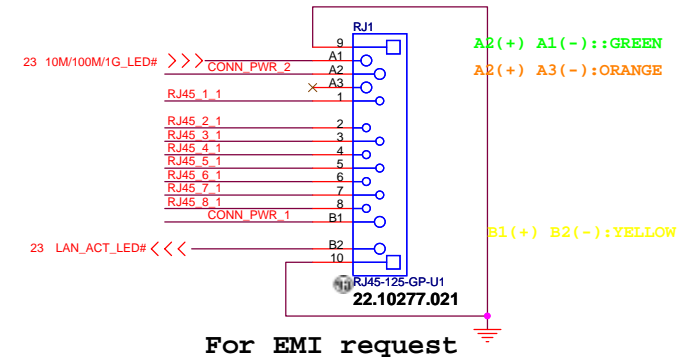
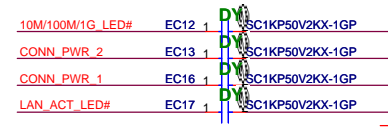
## ODD Connector



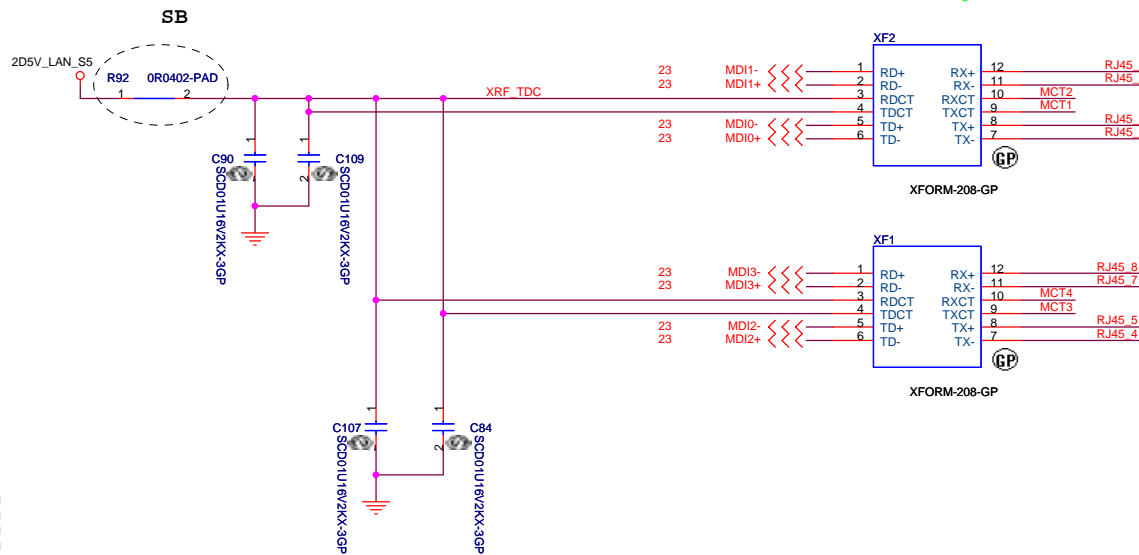
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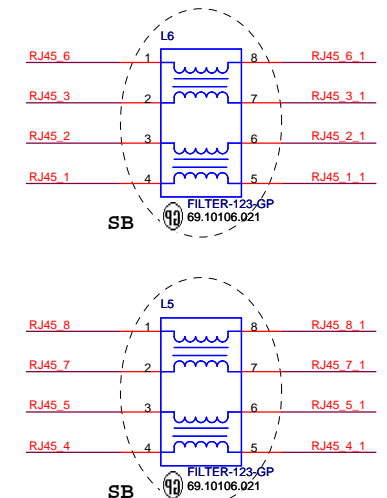
# LAN Connector



## GIGA Lan Transformer



For EMI request

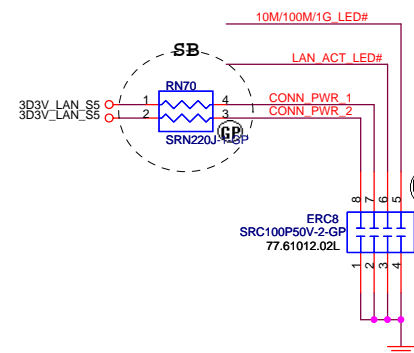
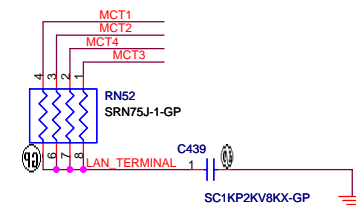


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

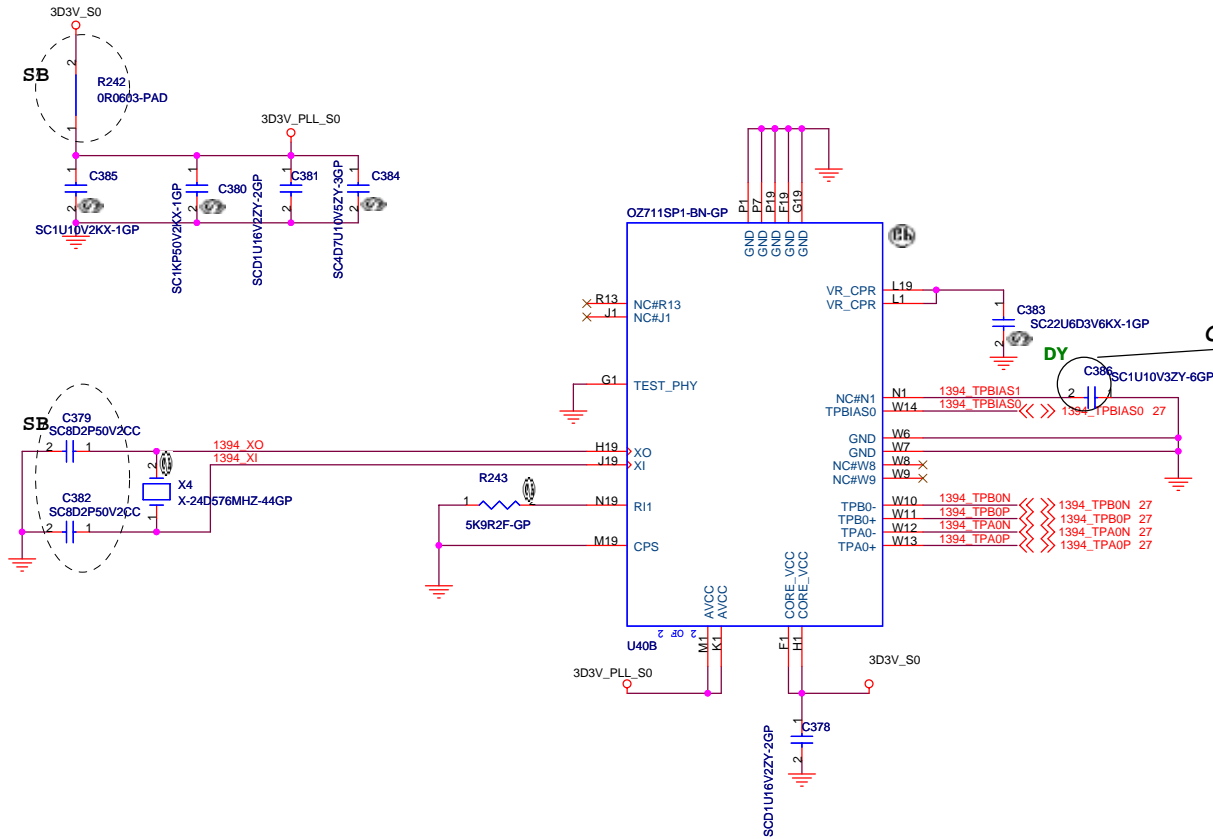


<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

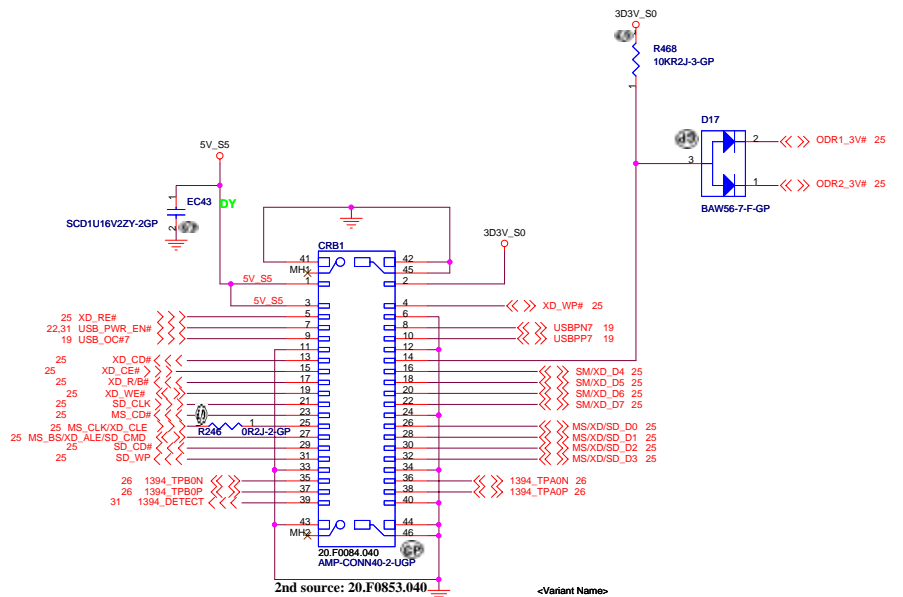
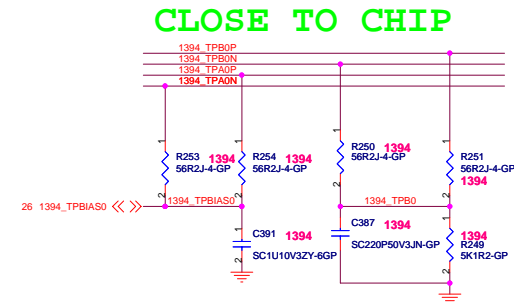
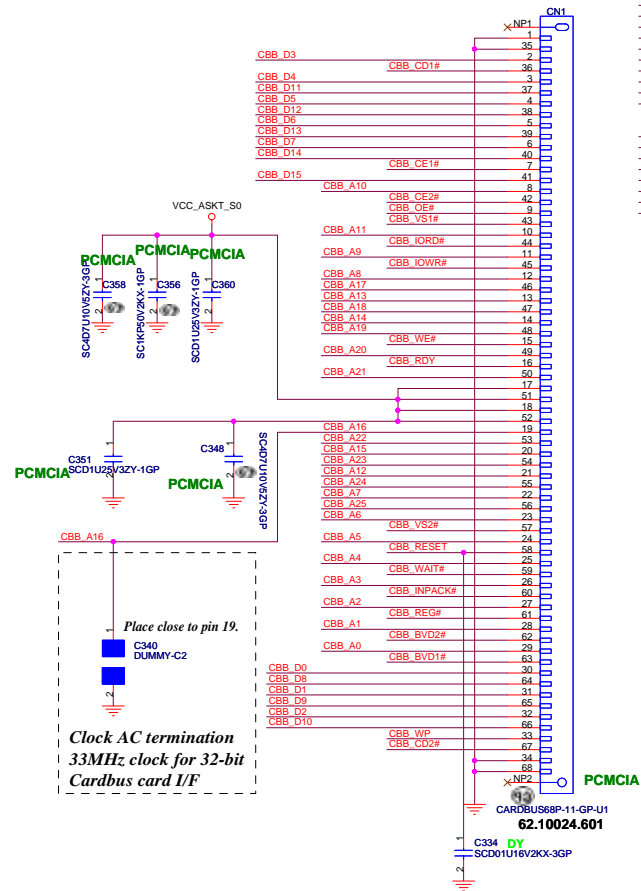
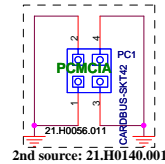
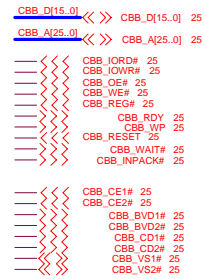
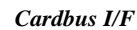
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Size	Document Number	Rev	SB
A3	Orta		
Date:	Friday, January 12, 2007	Sheet	24 of 46

Title			
OZ711SP1 (1 of 2)			
Size	Document Number		Rev
	Orta		SB
Date:	Friday, January 12, 2007	Sheet 25 of 46	




CHECK WITH FAE

### *PCMCIA Socket*

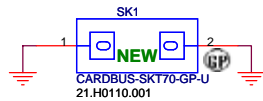


**XD  
MS / MS PRO  
SD / SD IO / MMC**

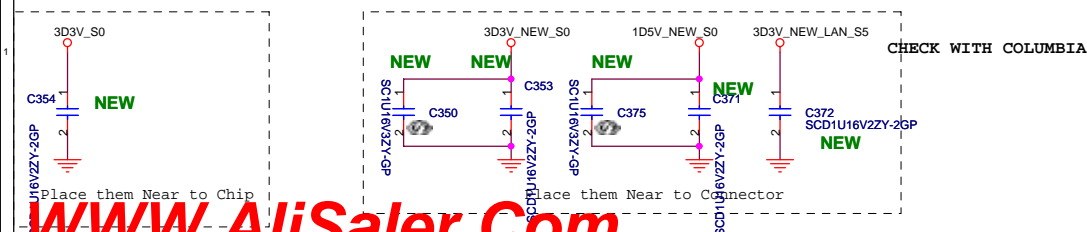
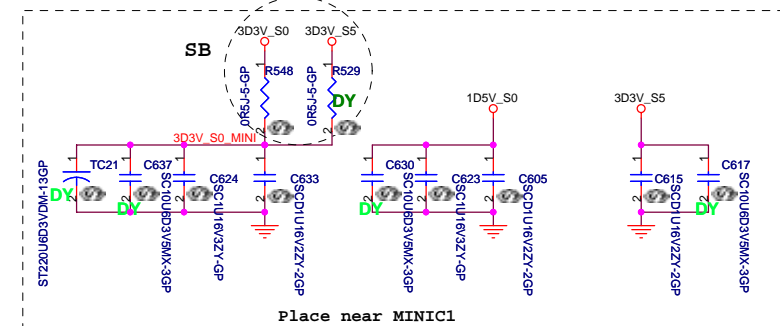
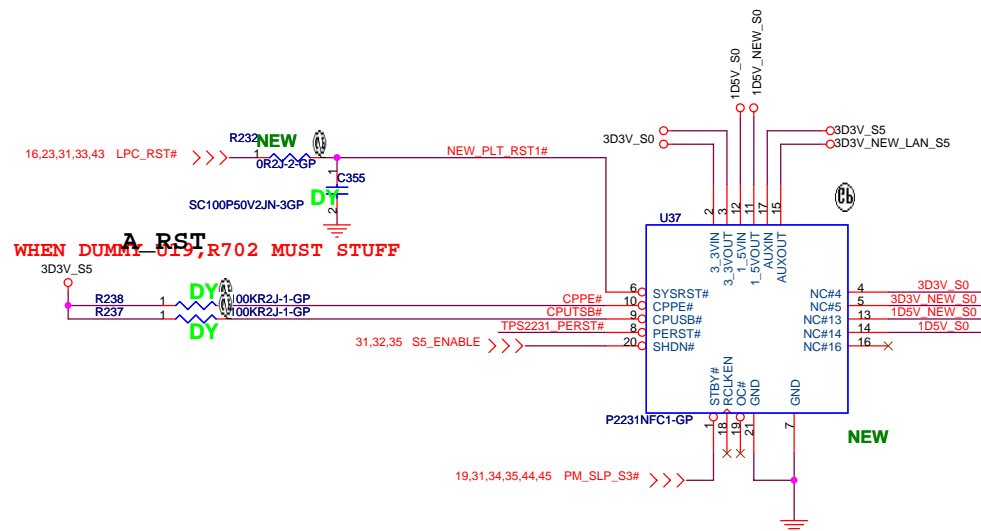
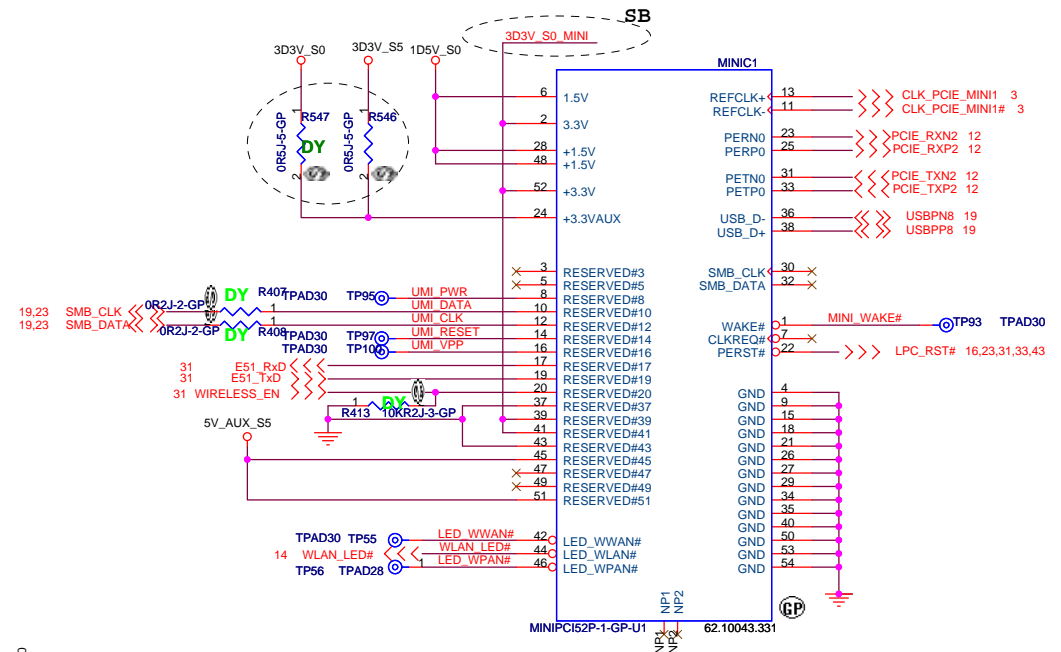
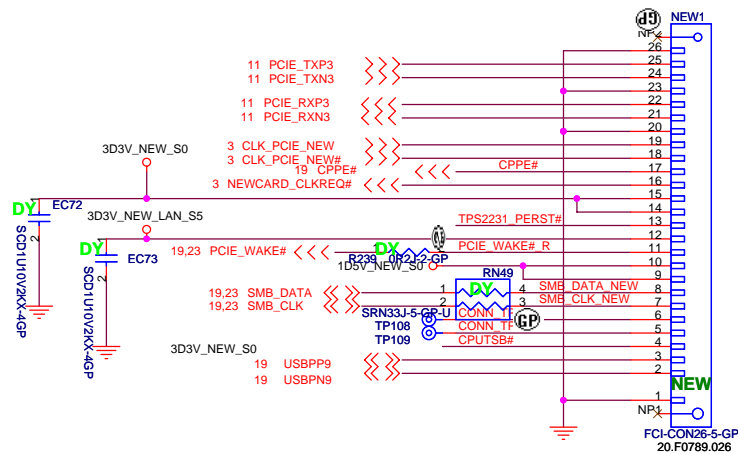
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Title					
<b>PCMCIA / 1394 / CARD READER</b>					
Size	Document Number				Rev
		<b>Orta</b>		<b>SB</b>	
Date:	Friday, January 12, 2007	Sheet	27	of	46

### *Mini Card Connector*

## NEWCARD Connector



Reserve the symbol  
for bottom side  
connector



**born1**

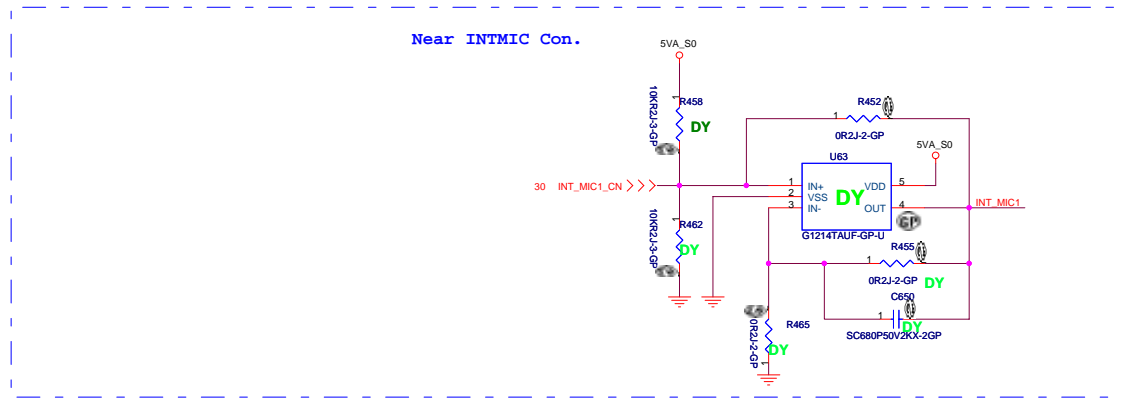
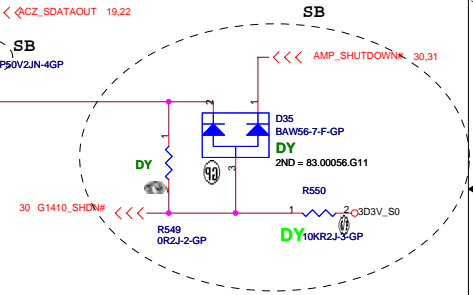
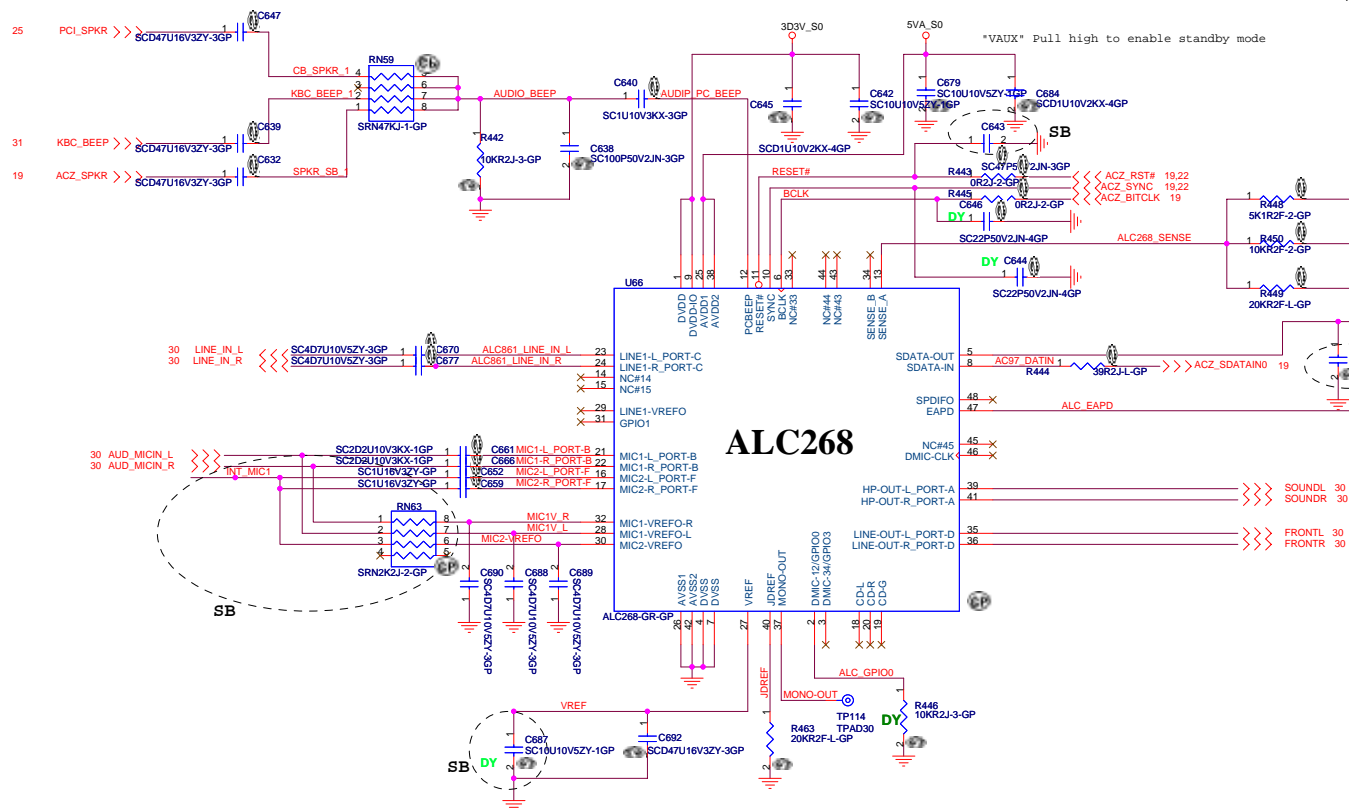
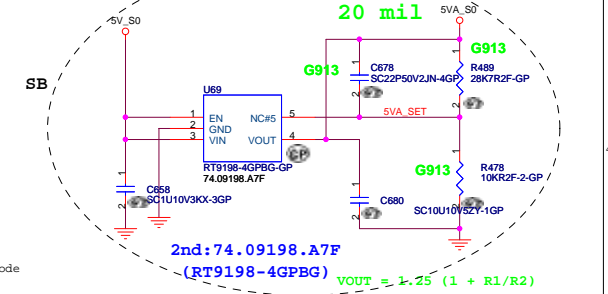
**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>MINI CARD / NEW CARD</b>			
Size	Document Number		Rev
	<b>Orta</b>		<b>SB</b>
Date:	Friday, January 12, 2007	Sheet 28 of 46	

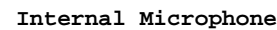
[www.AliSaler.Com](http://www.AliSaler.Com)

POWER GENERATE

\*Layout\*  
20 mil 5VA



## KBC\_MUTE\_GPIO8



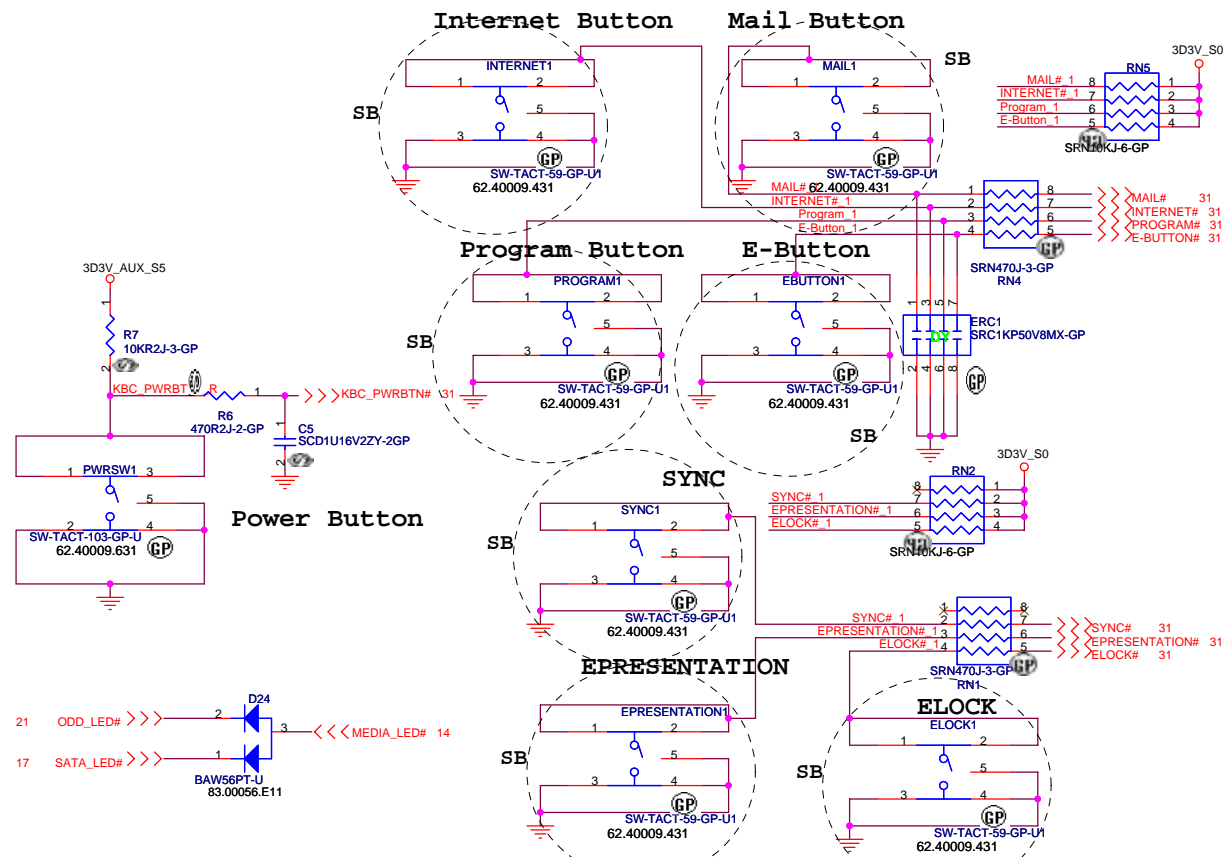
**Wistron Corporation**  
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### AUDIO AMP AND JACK

Orta

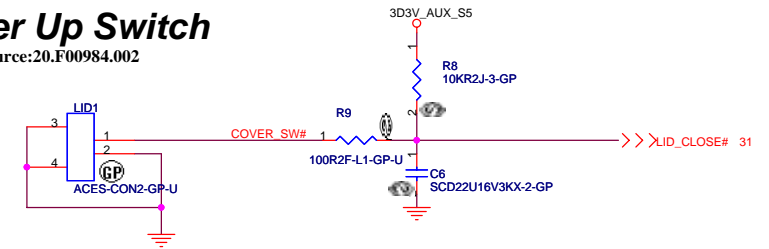
Rev	SB
-----	----



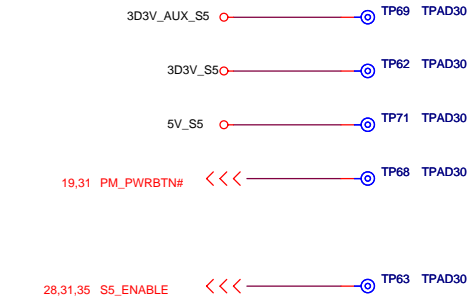


## Cover Up Switch

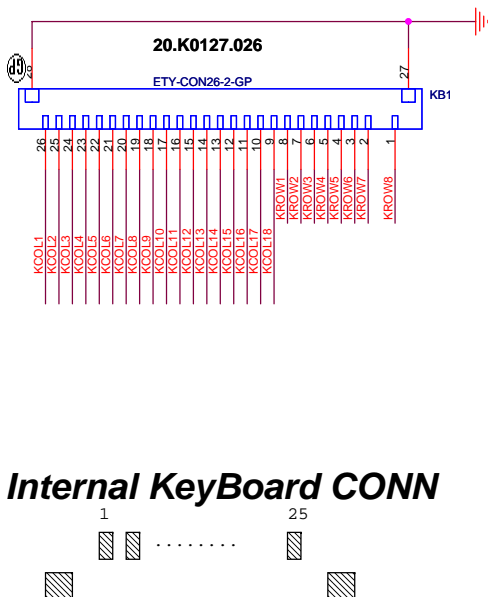
2nd source:20.F00984.002



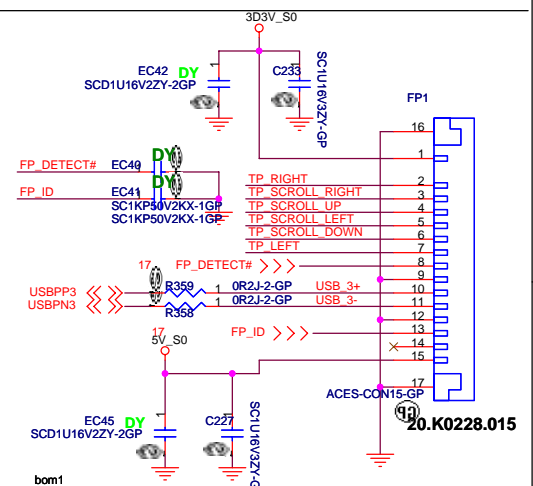
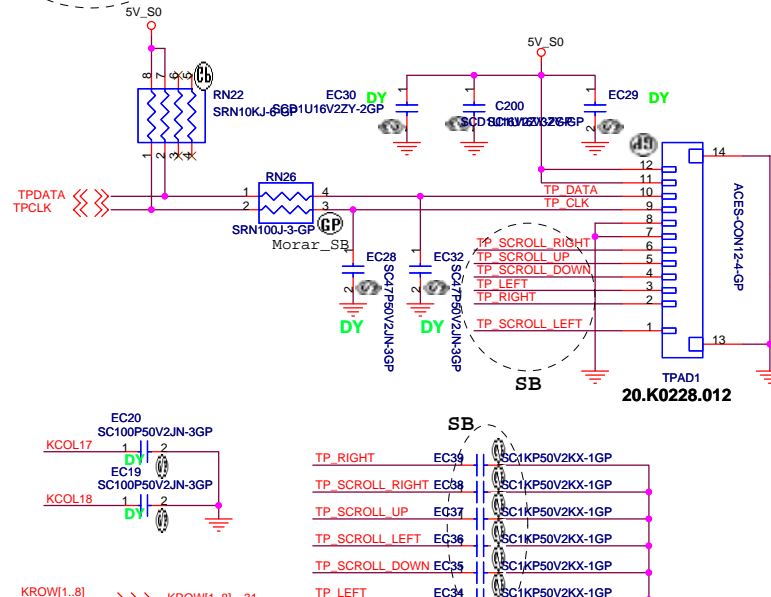
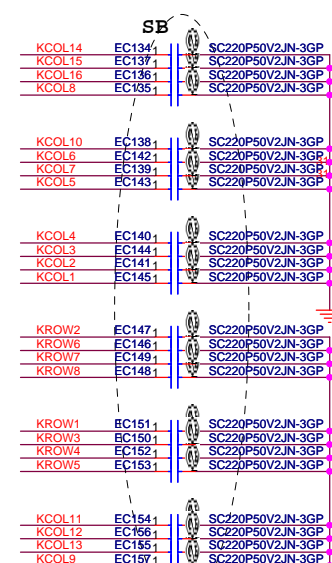
## Check test point



Test Point放在Dimm Door打開可量測處

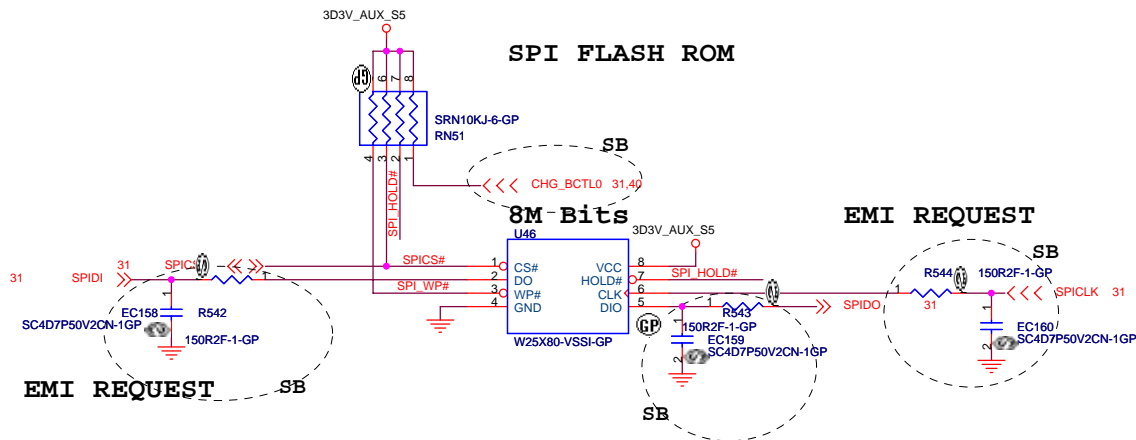


## EMI Bypass cap.



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Title		BUTTONS / KB / TOUCHPAD	
Size	Document Number	Rev	SB
Date:	Friday, January 12, 2007	Sheet	32 of 46



EMI REQUEST

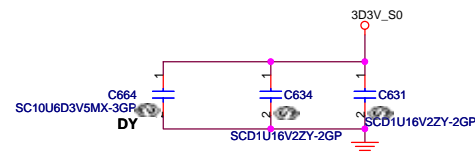
TOP VIEW

A15	(B1)
A14	(B2)
...	...
A2	(B14)
A1	(B15)

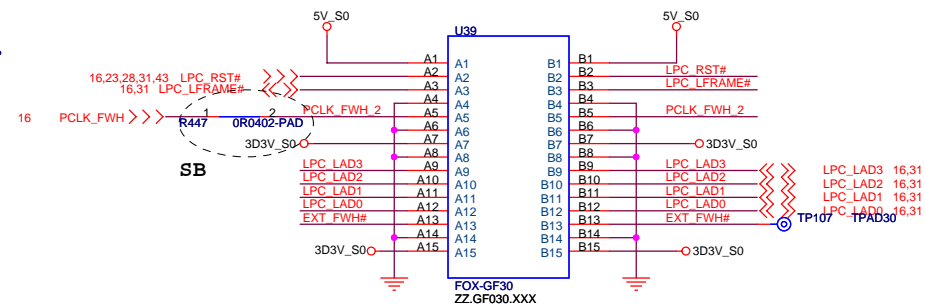
(BOTTOM VIEW)

EMI REQUEST

Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46

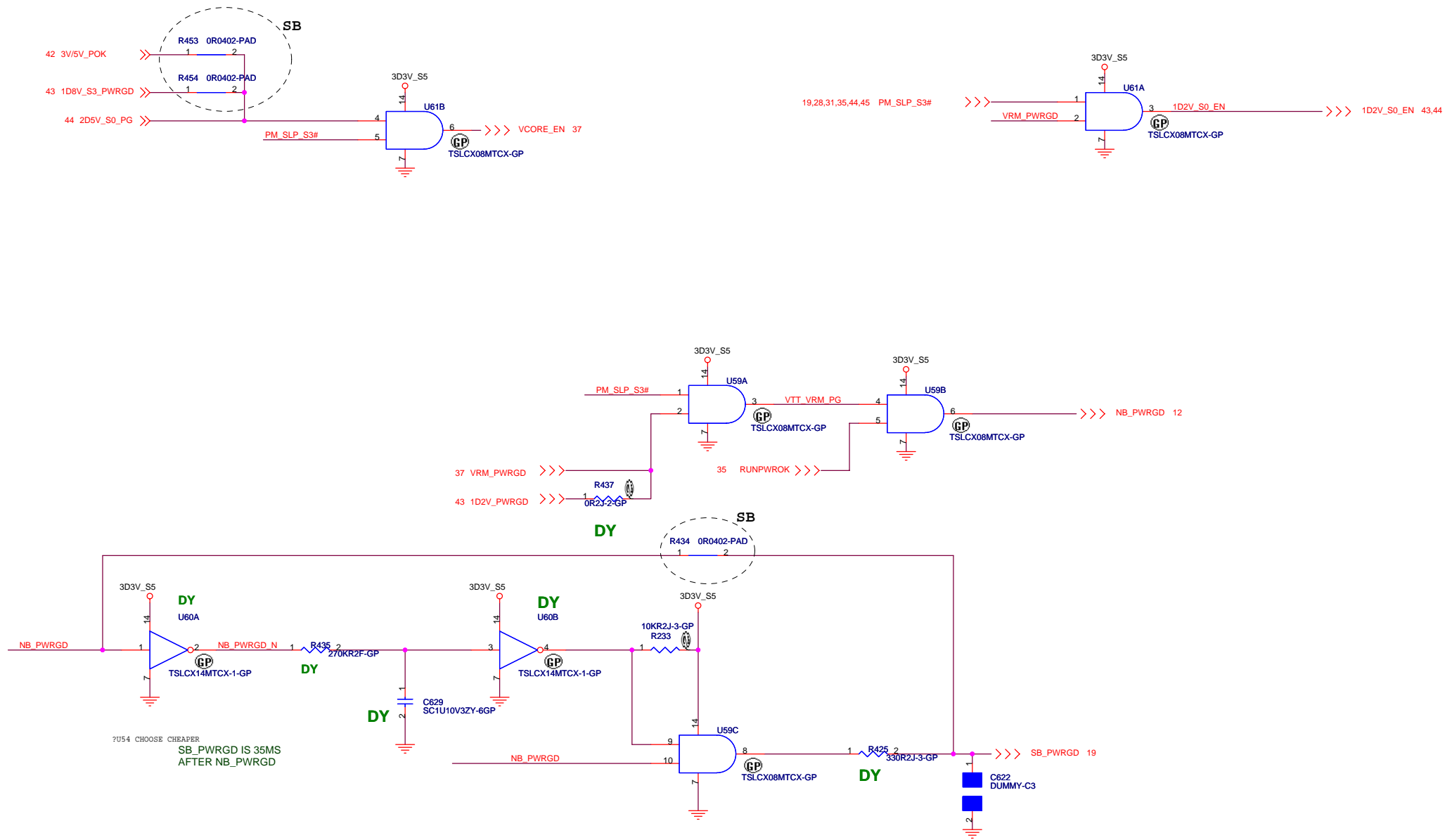


GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

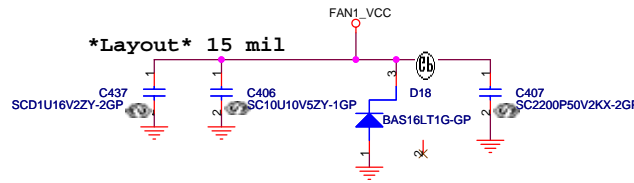
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
BIOS		
Size	Document Number	Rev
A3	Orta	SB
Date:	Friday, January 12, 2007	Sheet 33 of 46



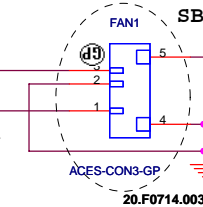
Setting T8 as 90 Degree

$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

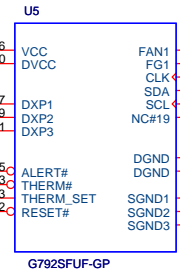
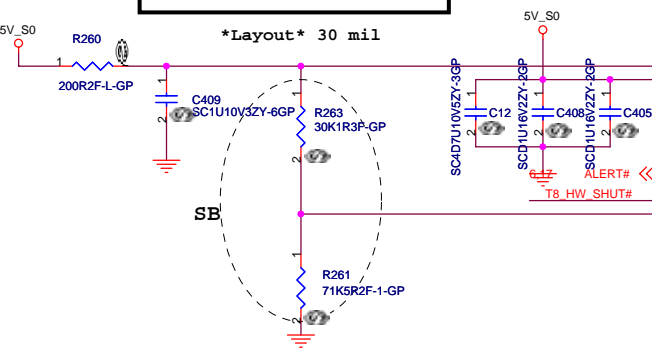
\*Layout\* 15 mil



\*Layout\* 15 mil



\*Layout\* 30 mil



DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

Place near chip as close as possible

2.System Sensor,  
Put between CPU and NB.

3.T8 Sensor

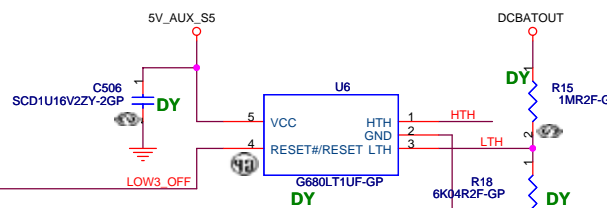
1.For CPU Sensor

Thermal Get Setting

Sensor	Setting	T6	T7
Sensor 1	CPU DTS	98	100
Sensor 2	G792-1 CPU	98	100
Sensor 3	G792-2 System	78	83

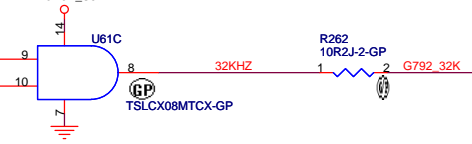
HW Thermal Throttling

BL3#



19,28,31,34,44,45 PM\_SLP\_S3#  
16 RTC\_CLK

32K suspend clock output



<Core Design>

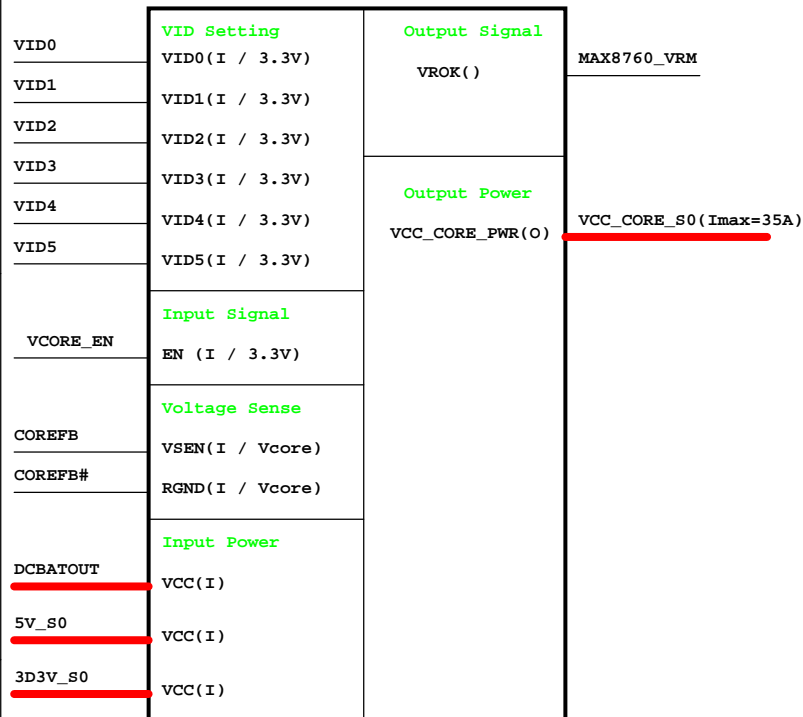
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **G792**

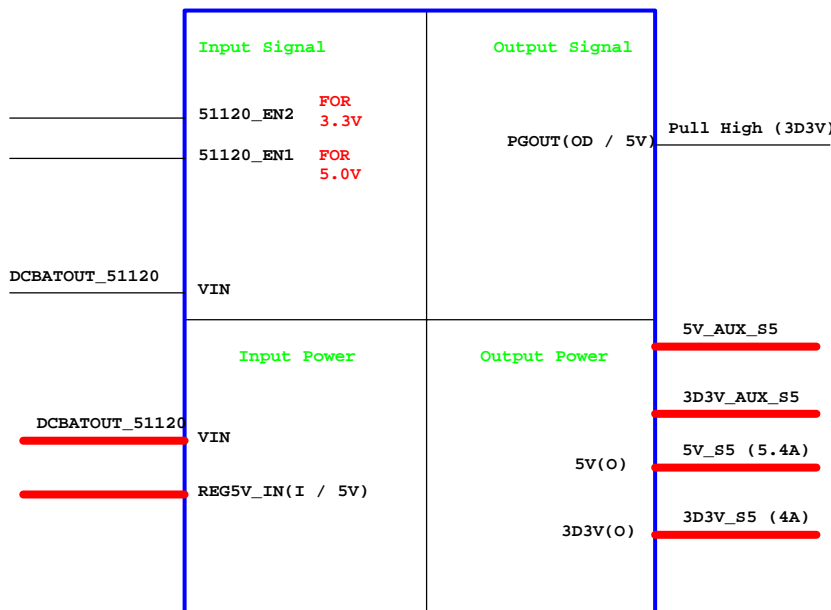
Size: A3 Document Number: Orta Rev: SB

Date: Friday, January 12, 2007 Sheet: 35 of 46

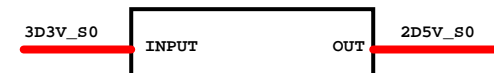
CPU\_CORE  
ISL6264CRZ



TI TPS51120  
3D3V/5V

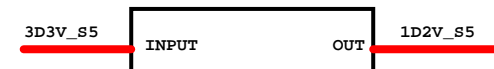


2D5V\_S0



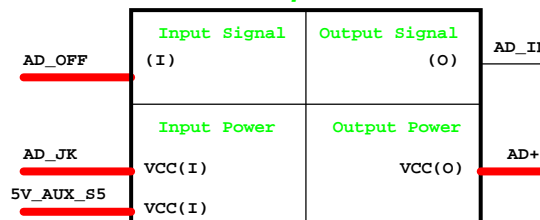
APL5913

1D8V\_S5

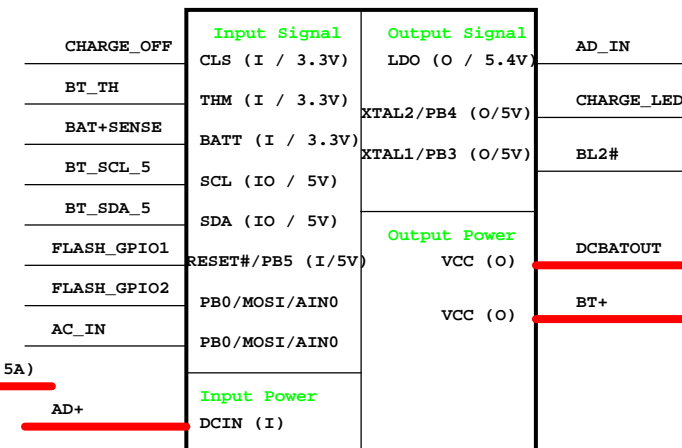


APL5332KAC-TRLGP

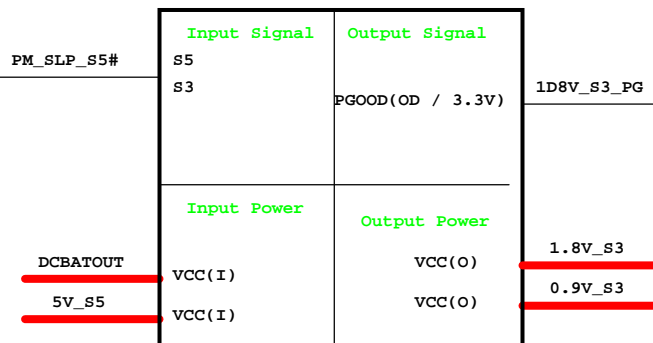
Adapter



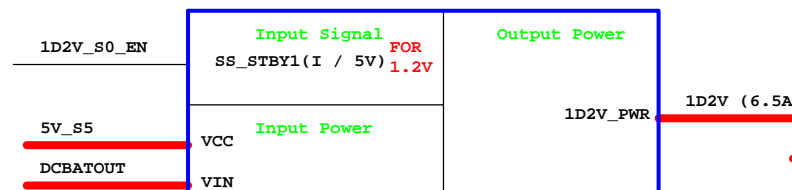
Charger\_ISL6255



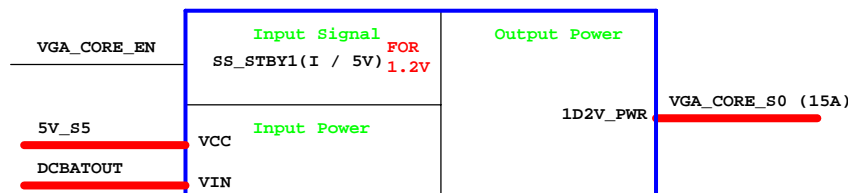
TI TPS51116  
1.8V / 0.9V



ISL6268\_1D2V



ISL6268\_VGA\_CORE

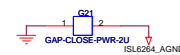


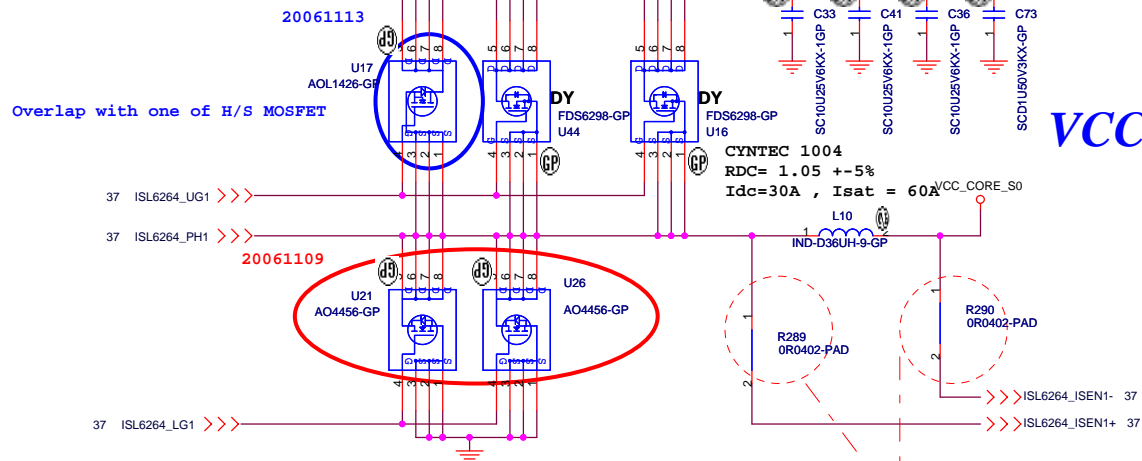
<Core Design>

<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p><b>Power Block Diagram</b></p>	
Size A3	Document Number
Date: Friday, January 12, 2007	Rev SB
Sheet 36 of 46	

VID=1.20V(25W)/1.15V(35W)  
Iomax=21A(25W)/35A (35W)  
OCP=40A~45A

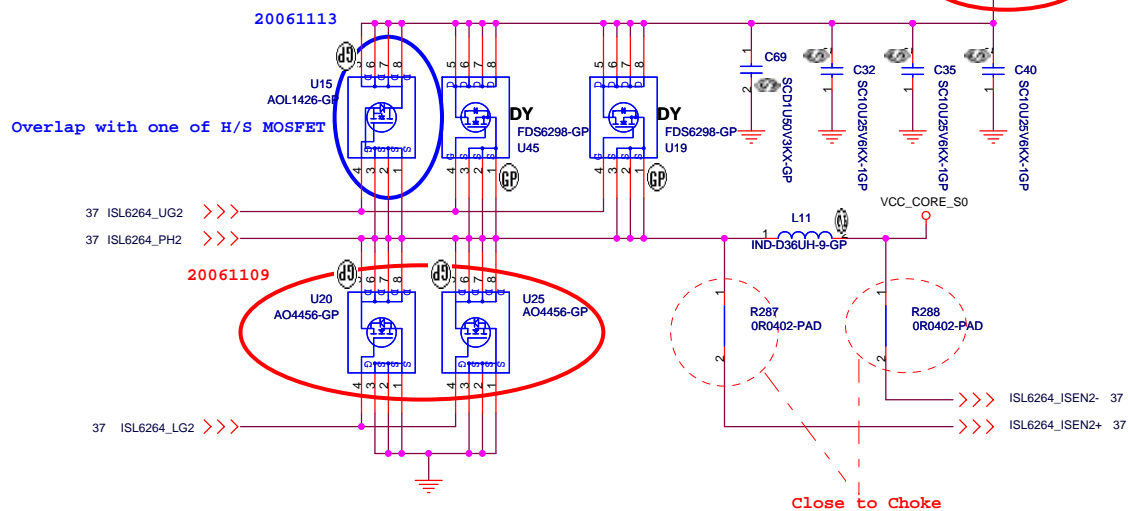
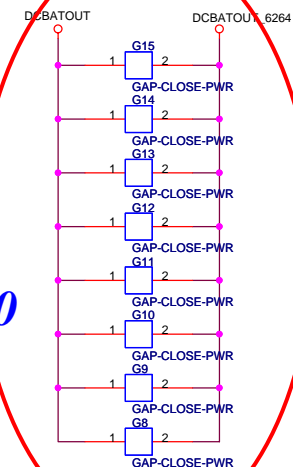
vDbs	vD4	vD3	vD2	vD1	vD0	bAc
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	1	1	1	0	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375





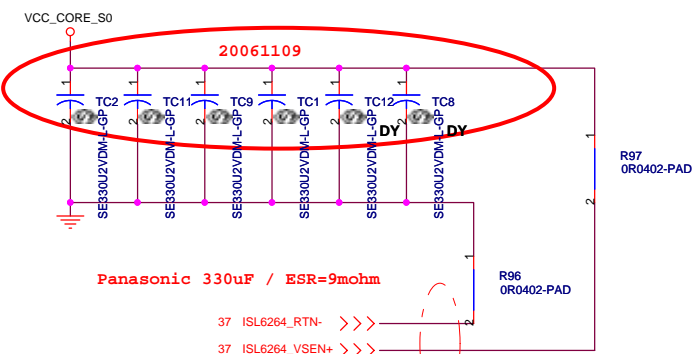
VCC\_CORE\_S0

20061109



Close to Choke

20061109



Close to Choke

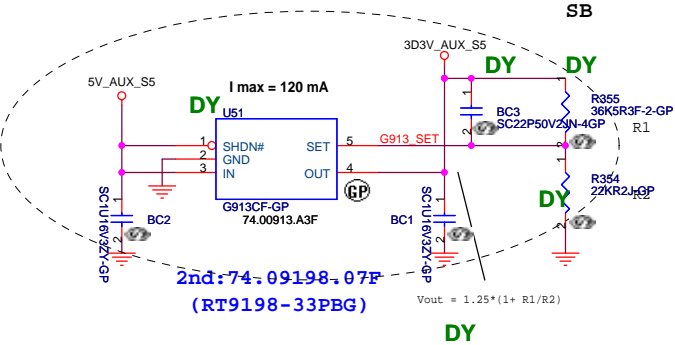
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Title			CPU Vcore Power_2	
Size	Document Number	Rev		SB
A3		Orta		
Date:	Friday, January 12, 2007	Sheet	38	of 46

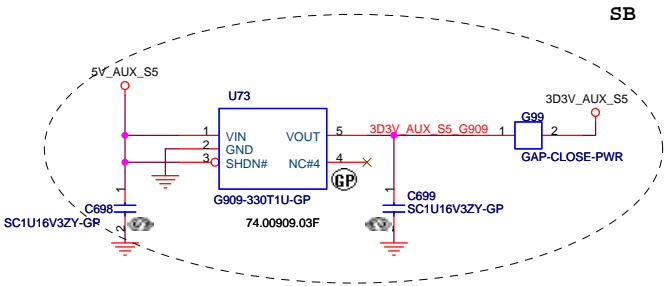
Aux Power

3D3V\_AUX\_S5



Aux Power

3D3V\_AUX\_S5

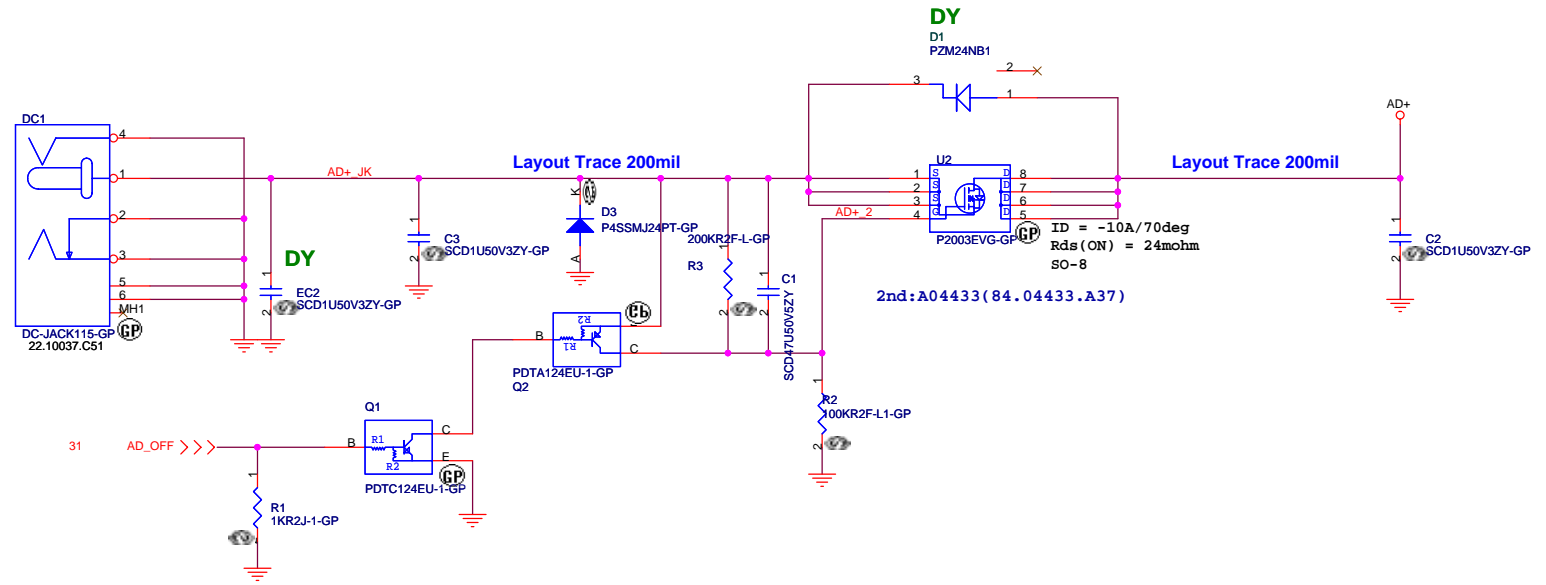


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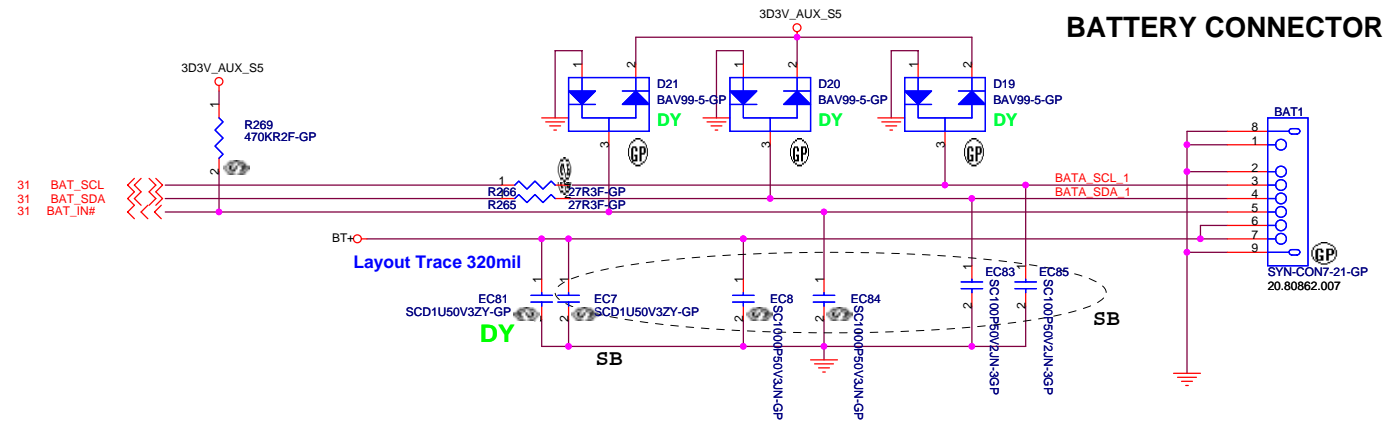
<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Title			
<b>3D3V_AUX</b>			
Size	Document Number		Rev
A3	Orta		SB
Date:	Friday, January 12, 2007		
Sheet	39	of	46



## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR

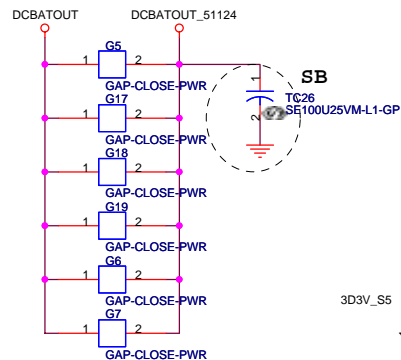


<Variant Name>

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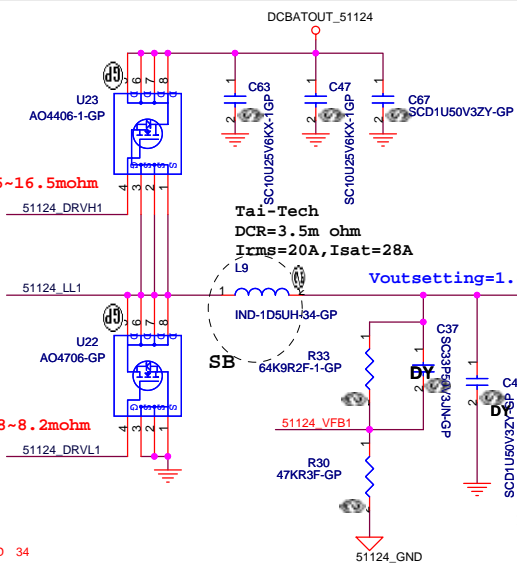
Title			
<b>AD/BATT CONN</b>			
Size A3	Document Number		Rev
	<b>Orta</b>		<b>SB</b>
Date:	Friday, January 12, 2007	Sheet 41 of	46





$I_d=9.6A$   
 $Q_g=18\sim nC$ ,  
 $R_{dson}=13.5\sim 16.5m\Omega$

$I_d=13.2A$   
 $Q_g=27nC$ ,  
 $R_{dson}=6.8\sim 8.2m\Omega$

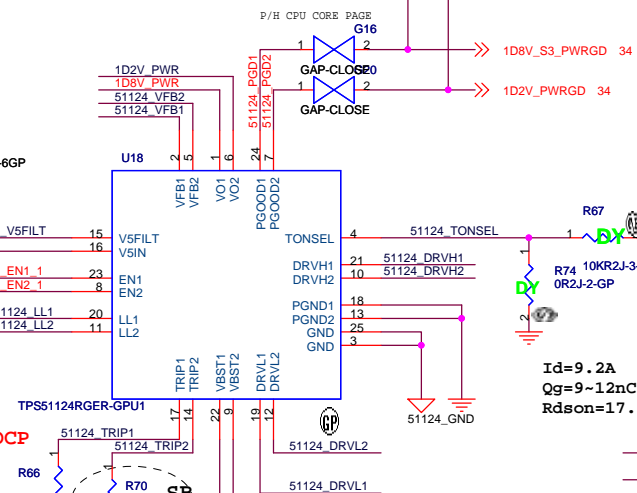


**1D8V Iomax=8A**  
**OCP>16A**

**Nippon Chemi-Con**  
**Al Cap.**  
**390uF/2D5V**  
**ESR=15mohm**

**Kemet**  
**220uF/ 4V**  
**ESR=15mohm**

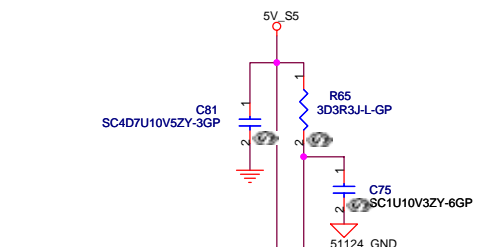
$$V_{out}=0.758V \cdot (R1+R2)/R2$$



**1D2V Iomax=8A**  
**OCP>16A**

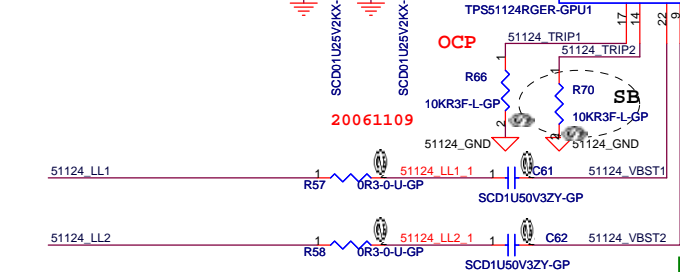
**Nippon Chemi-Con**  
**Al Cap.**  
**390uF/2D5V**  
**ESR=15mohm**

**Kemet**  
**220uF/ 4V**  
**ESR=15mohm**



19,31.44 PM\_SLP\_S5#  
 34.44 1D2V\_S0\_EN

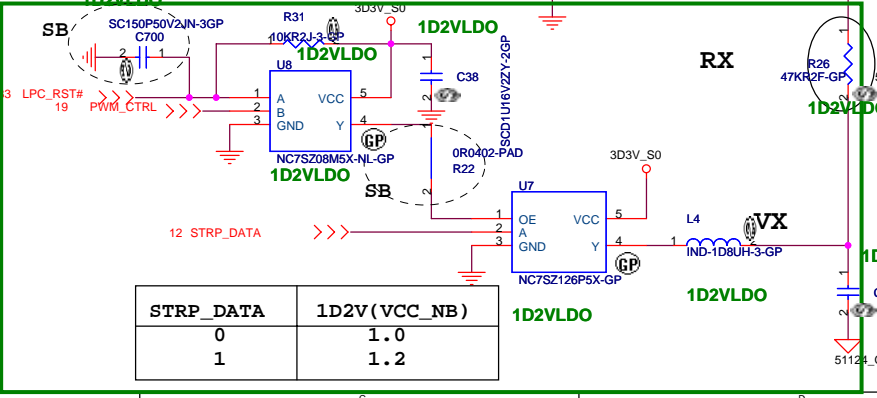
20061113



$$V_{trip}(mV)=R_{trip}(K\Omega) \cdot 10(uA)$$

$$I_{ocp}=(V_{trip}/R_{dson})+((1/(2 \cdot L \cdot f)) \cdot ((V_{in}-V_{out}) \cdot V_{out})/V_{in}))$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2



STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

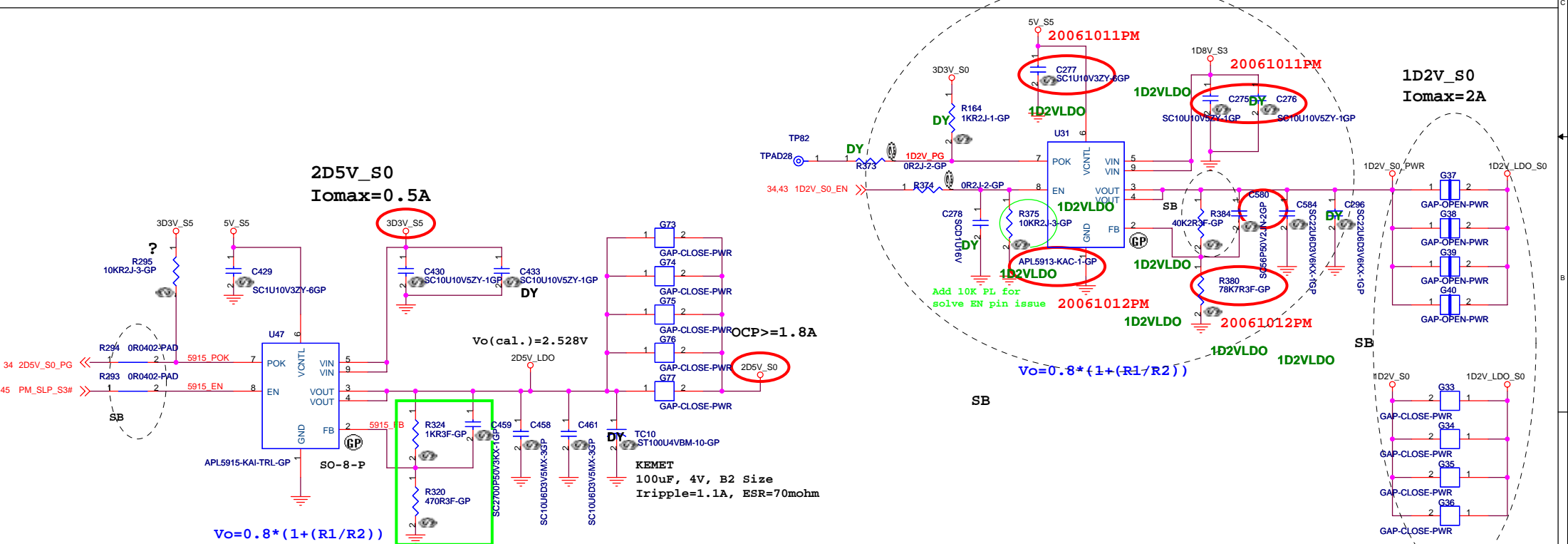
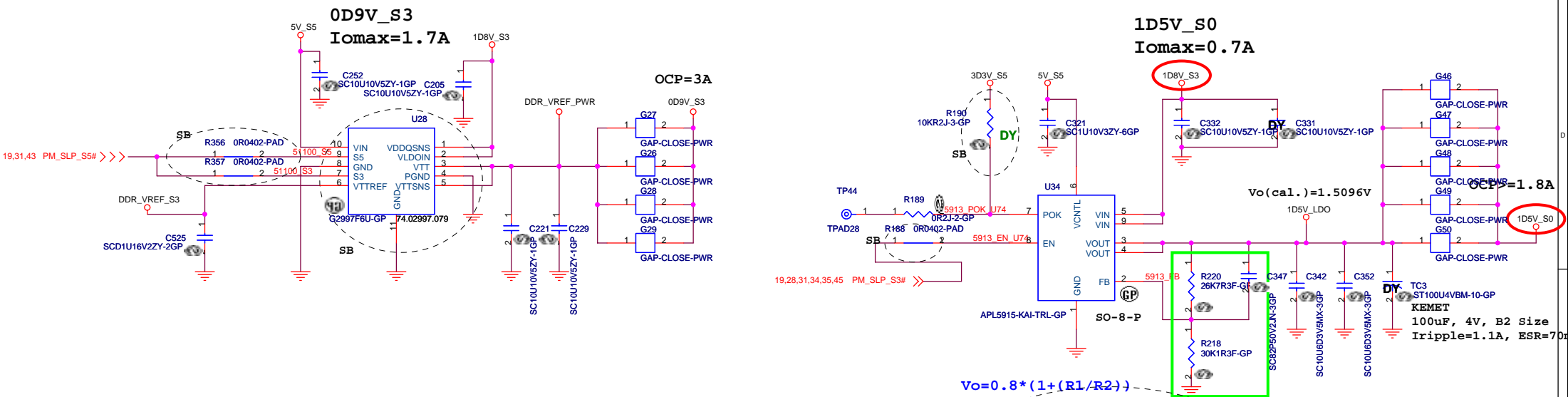
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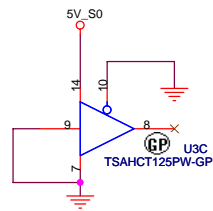
**TPS51124 1D8V 1D2V**

Rev **SB**

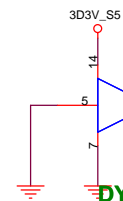
Date: Friday, January 12, 2007 Sheet 43 of 46



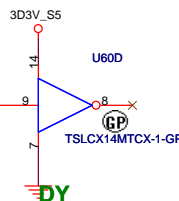




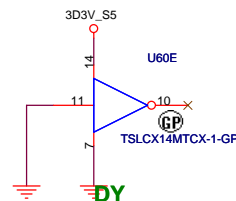
DUMMY in SA



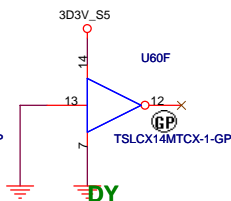
34.42Y01.001



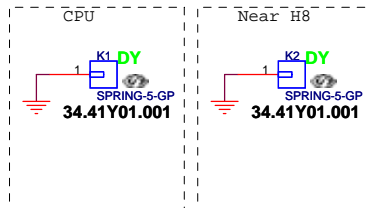
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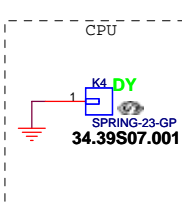
34.4G502.001



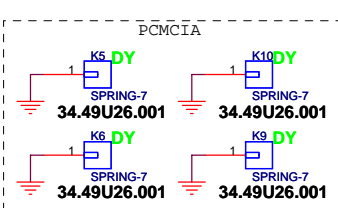
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34.42Y01.001

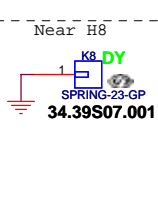


34.39S07.001

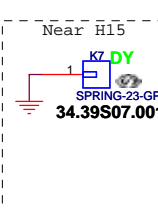


34.49U26.001

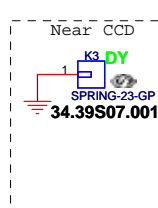
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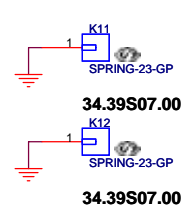
34.39S07.001



34.39S07.001



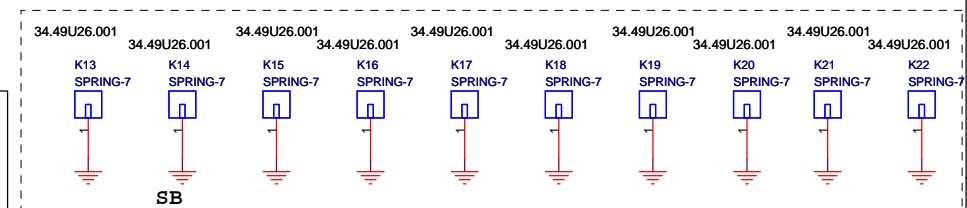
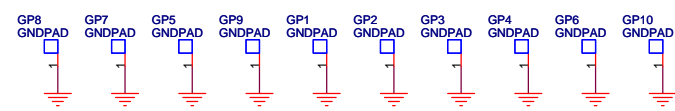
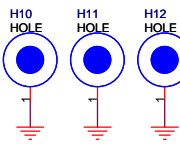
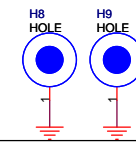
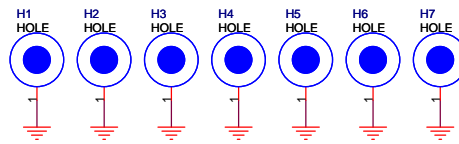
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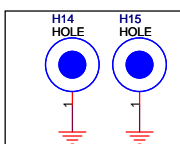
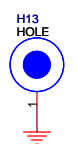
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34.39S07.001

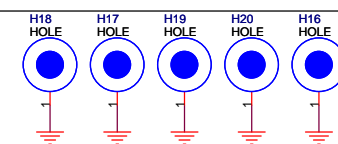
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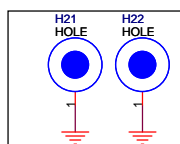
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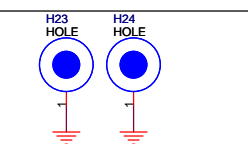
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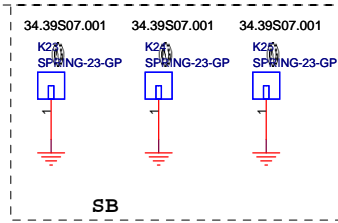
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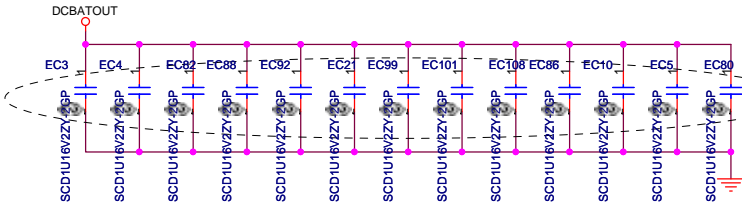
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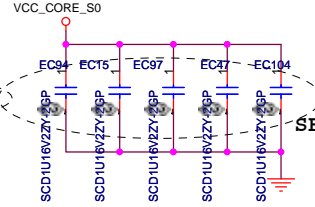
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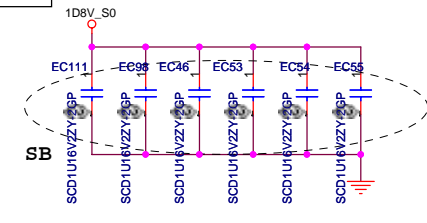
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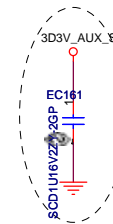
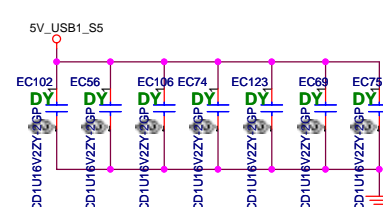
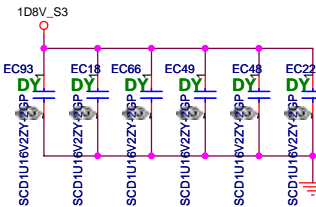
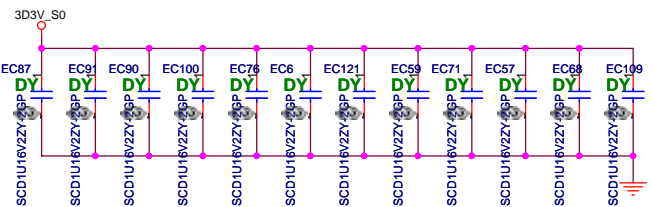
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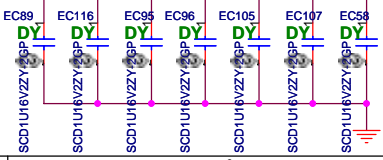
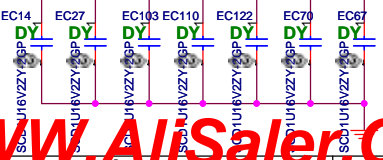
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<Core Design>

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Title		EMI/Spring/Boss	
Size	Document Number	Rev	SB
Date: Friday, January 12, 2007		Sheet 46 of 46	